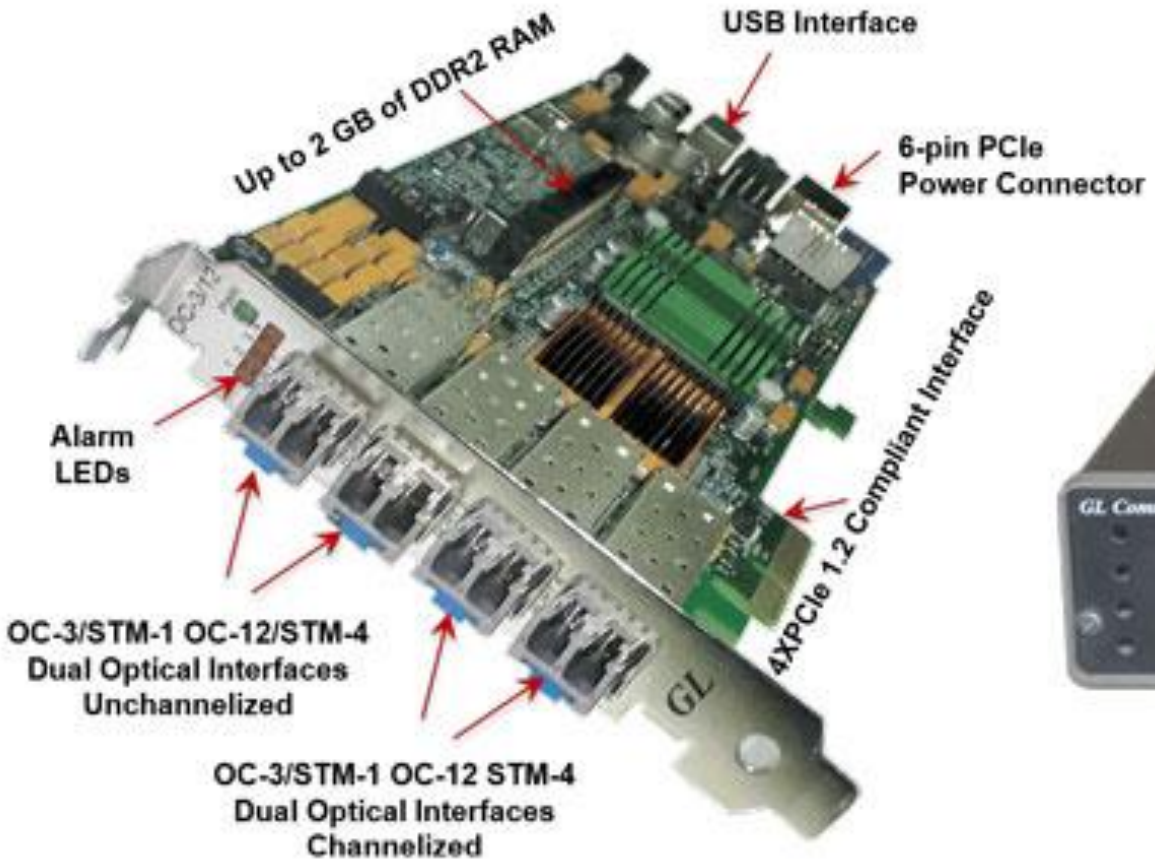
ATM BERT

GL Communications Inc.
818 West Diamond Avenue - Third Floor, Gaithersburg, MD 20878
Phone: (301) 670-4784 Fax: (301) 670-9187 Email: info@gl.com
Website: https://www.gl.com

OC-3 / STM-1 and OC-12 / STM-4 Platforms



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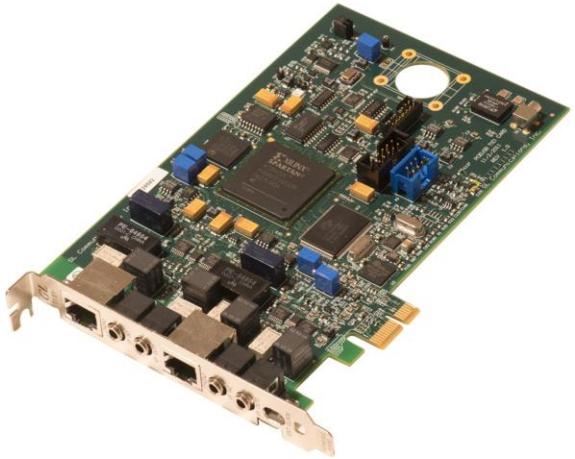
T1 E1 Platforms

Front Panel

Back Panel

tProbe™ - Portable USB based T1 E1 VF FXO FXS and Serial Datacom Analyzer

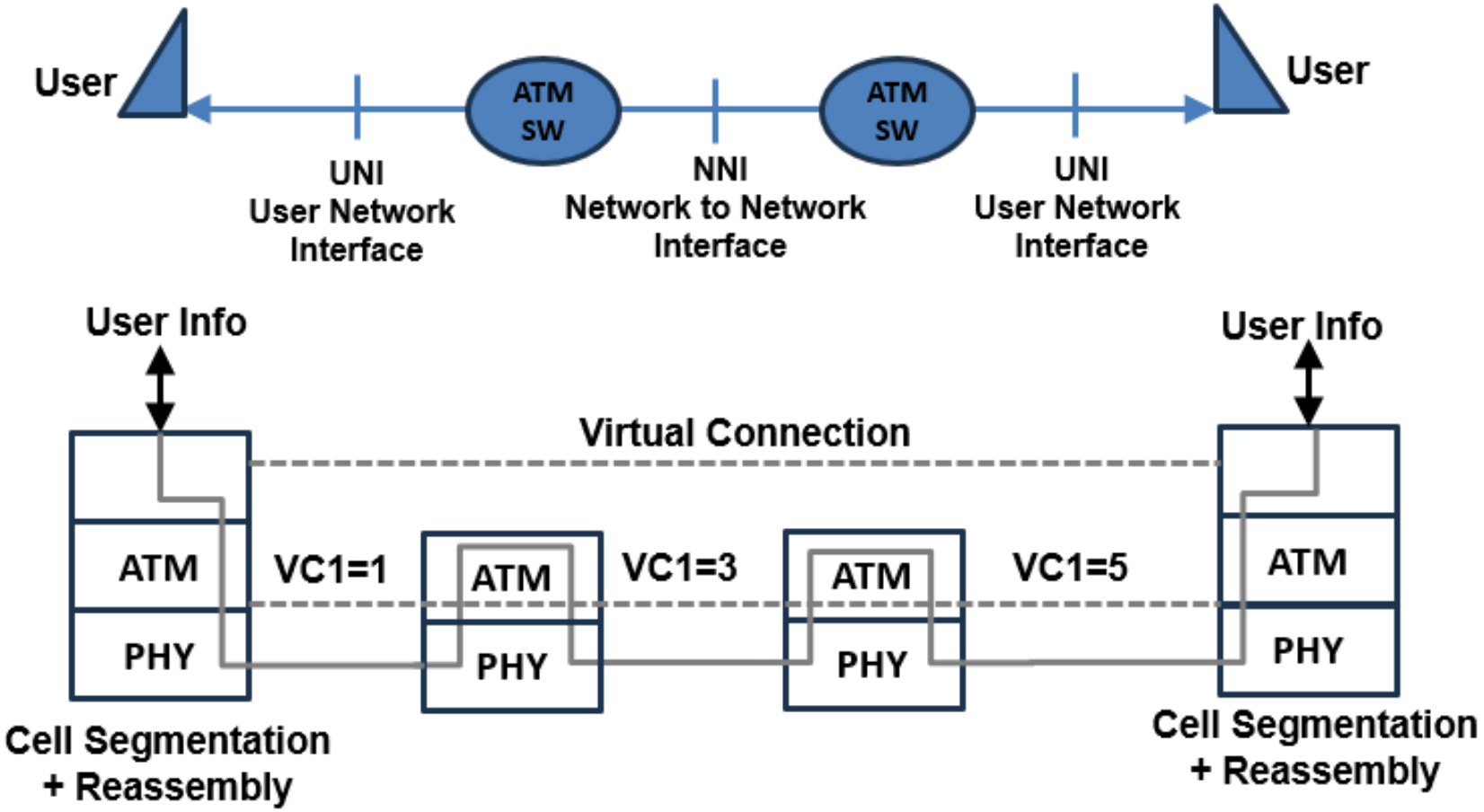
Quad / Octal T1 E1 PCIe Card



Dual T1 E1 Express (PCIe) Board

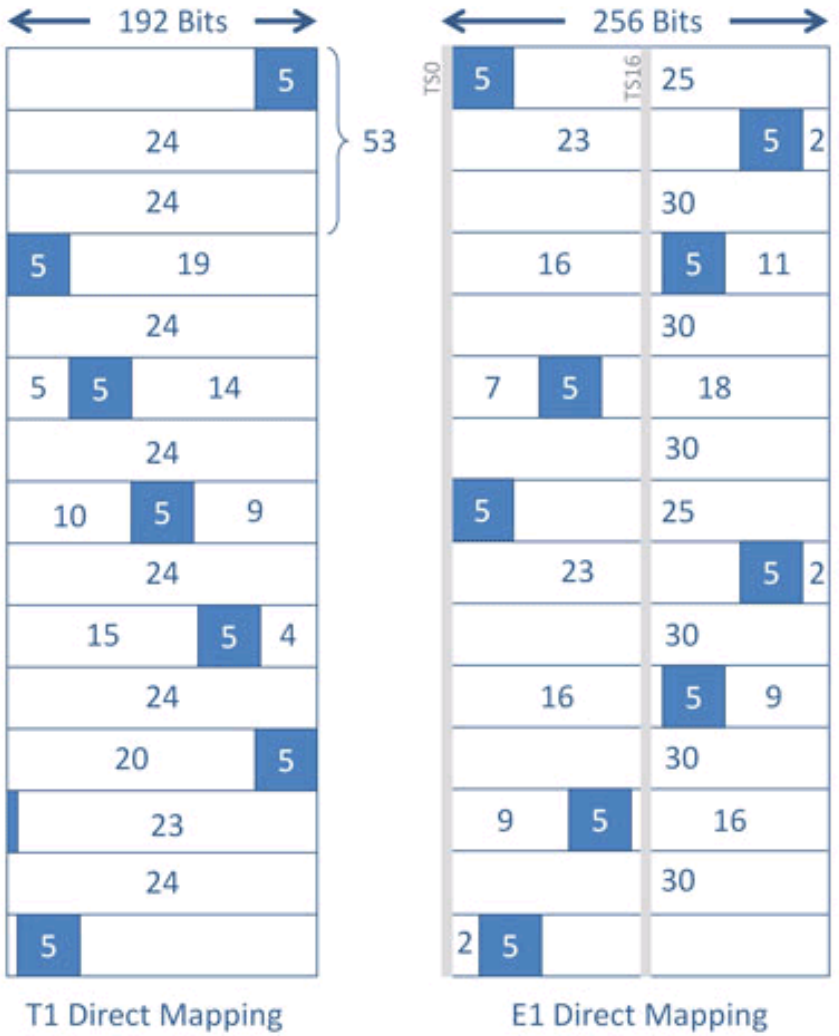
tScan16™ with
16-port T1 E1 Breakout Box

A Typical ATM Circuit

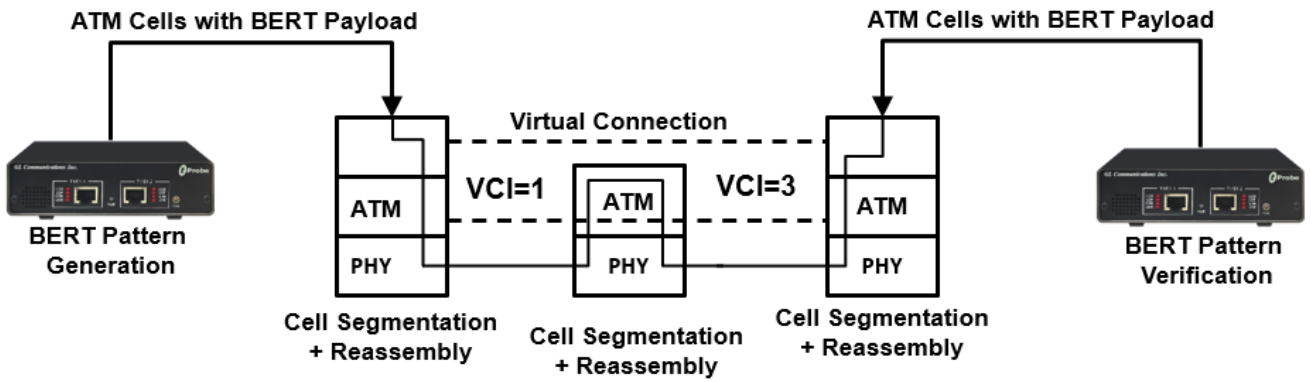


- ATM BERT: A typical ATM BERT application is the verification of end-to-end integrity in an ATM virtual connection

T1 and E1 ATM Direct Mapping



ATM BERT



- Capable of generating /receiving traffic
- Support user-defined ATM header configuration for GFC, VPI, VCI, PT, CLP
- User-defined traffic rate to the accuracy of 1% of total bandwidth
- Supports different QRSS, PRBS patterns 2^9-1, 2^{11}-1, 2^{15}-1, 2^{20}-1, 2^{23}-1, All one's, All zero's, alternate 1's and 0's, 1:1, 1:7, and User - defined pattern (ranging between 3 to 32 bits)
- Supports inverting, and scrambling payload data. Scrambling is according to ITU-T G.804
- Supports single bit error insertion, and error rate insertion
- Provides ATM QoS measurement (bit error count/ rate/seconds, sync Loss, no rx data etc.)
- Provides ATM Statistics (total cell count, rejected / pass / idle cell counts, cell rate, and HEC error count)
- Provides throughput details, error, and alarm LEDs for easy analysis
- Supports testing on multiple cards simultaneously with consolidated result view
- Tx and Rx settings for multiple cards can be independently controlled or coupled
- Capable to save and load the configuration settings

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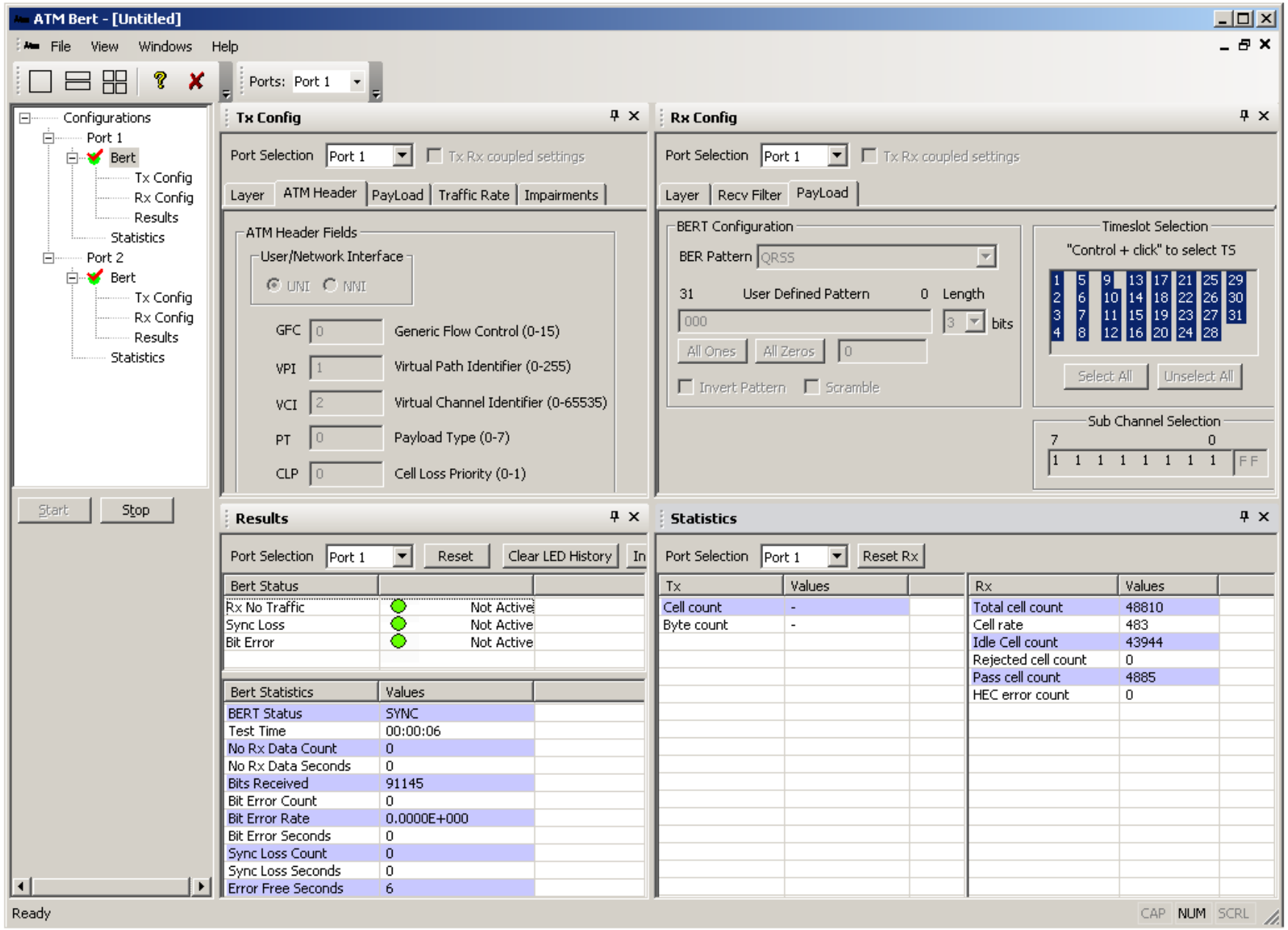
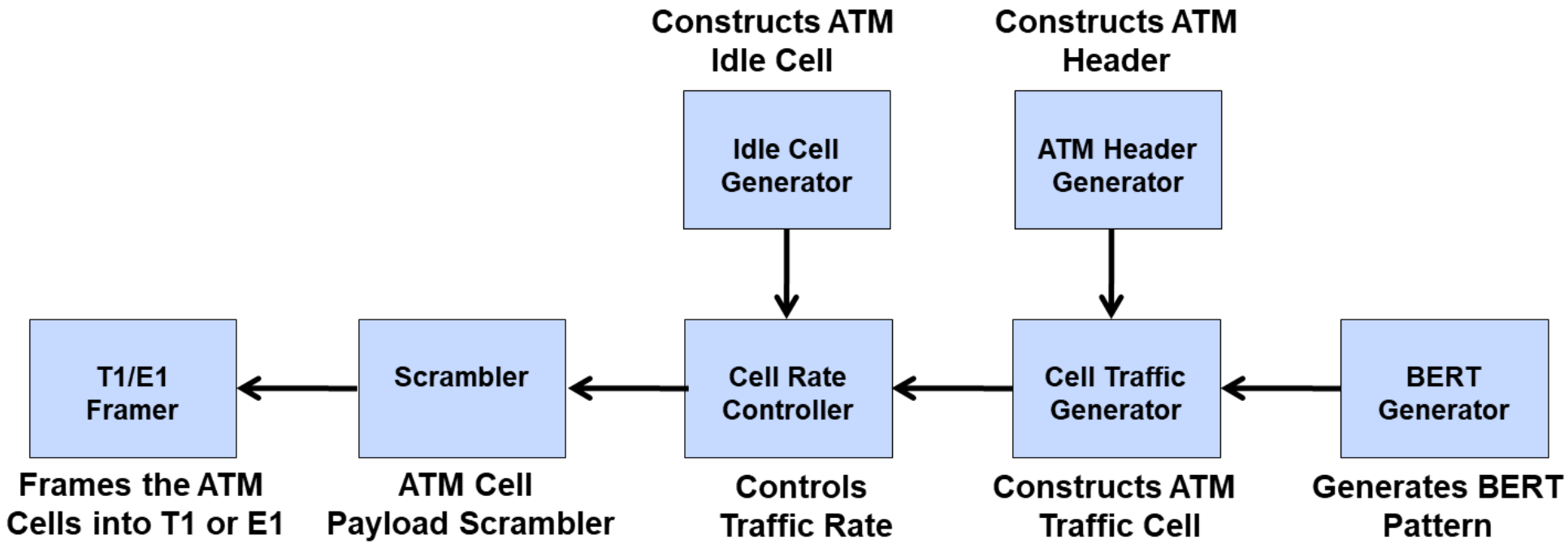
ATM BERT GUI


ATM Bert - [Untitled]
File View Windows Help
Ports: Port 1
Configurations
Port 1
Bert
Tx Config
Rx Config
Results
Statistics
Port 2
Bert
Tx Config
Rx Config
Results
Statistics
Start
Stop
Tx Config
Port Selection Port 1
Tx Rx coupled settings
Layer ATM Header PayLoad Traffic Rate Impairments
ATM Header Fields
User/Network Interface
UNI NNI
GFC 0 Generic Flow Control (0-15)
VPI 1 Virtual Path Identifier (0-255)
VCI 2 Virtual Channel Identifier (0-65535)
PT 0 Payload Type (0-7)
CLP 0 Cell Loss Priority (0-1)
Rx Config
Port Selection Port 1
Tx Rx coupled settings
Layer Recv Filter PayLoad
BERT Configuration
BER Pattern QRSS
31 User Defined Pattern 0 Length
000
3 bits
All Ones All Zeros 0
Invert Pattern Scramble
Timeslot Selection
"Control + click" to select TS
1 5 9 13 17 21 25 29
2 6 10 14 18 22 26 30
3 7 11 15 19 23 27 31
4 8 12 16 20 24 28
Select All Unselect All
Sub Channel Selection
7 0
1 1 1 1 1 1 1 1 FF
Results
Port Selection Port 1 Reset Clear LED History In
Bert Status
Rx No Traffic Not Active
Sync Loss Not Active
Bit Error Not Active
Bert Statistics Values
BERT Status SYNC
Test Time 00:00:06
No Rx Data Count 0
No Rx Data Seconds 0
Bits Received 91145
Bit Error Count 0
Bit Error Rate 0.0000E+000
Bit Error Seconds 0
Sync Loss Count 0
Sync Loss Seconds 0
Error Free Seconds 6
Statistics
Port Selection Port 1 Reset Rx
Tx Values
Cell count -
Byte count -
Rx Values
Total cell count 48810
Cell rate 483
Idle Cell count 43944
Rejected cell count 0
Pass cell count 4885
HEC error count 0
Ready
CAP NUM SCRL

Tx and Rx Configuration

- Tx configuring allows to configure the parameters in the Tx direction i.e., outgoing traffic
- **Tx Config** option allows -
  - Configuring ATM Header fields
  - Configuring various BERT patterns
  - Applying traffic type
  - Invert BER patterns
  - Scrambling
  - Single bit error insertion or error rate insertion
- Rx configuration allows to configure the parameters for the Rx direction i.e., incoming traffic. Rx parameters are used to compare against incoming traffic and perform BERT measurements
- **Rx Config** option allows configuring –
  - ATM Header fields
  - BERT Patterns
  - Receive Filters

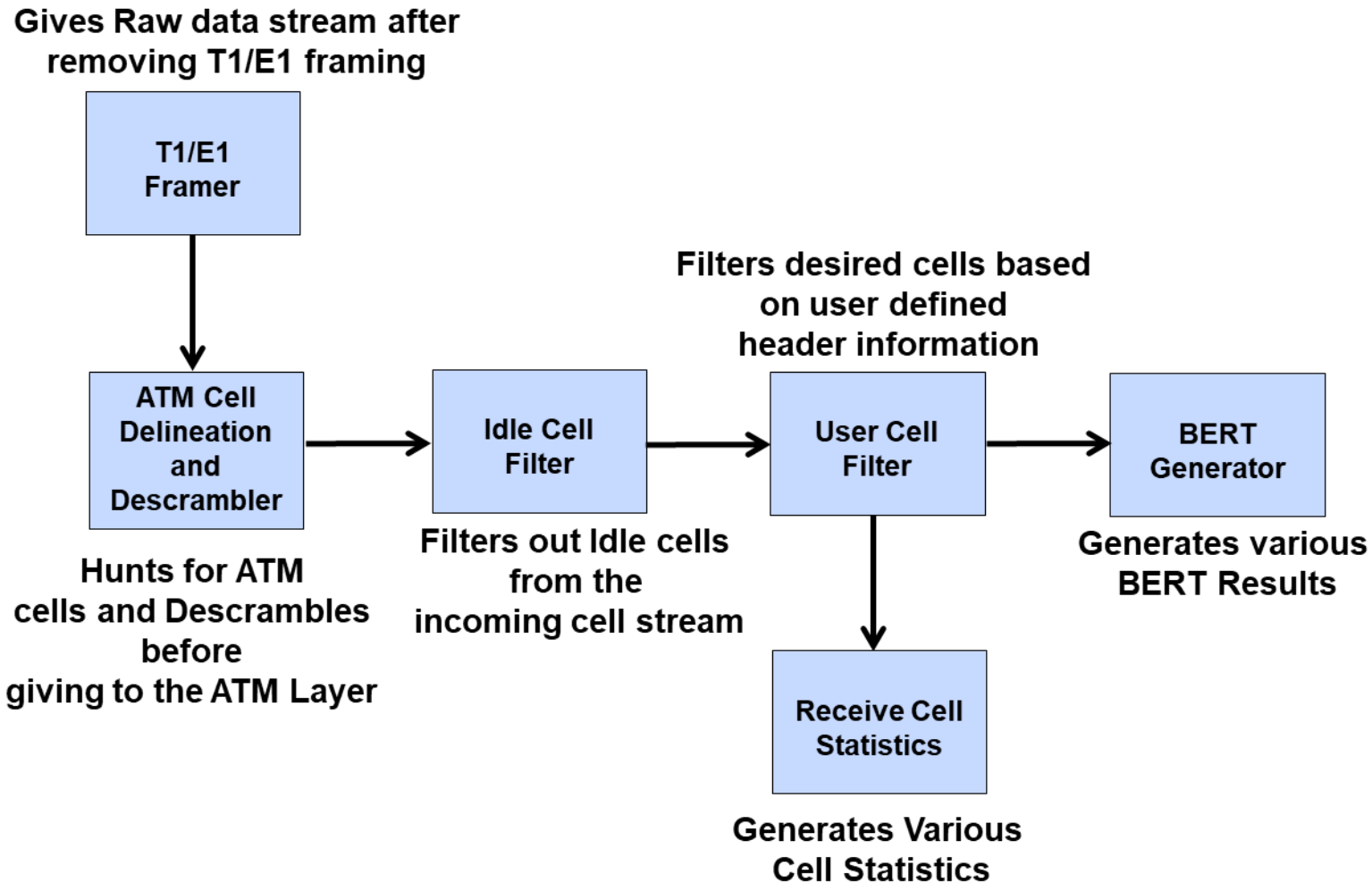
Transmit ATM Block Diagram



Description of Transmit ATM Blocks

- BERT GENERATOR – This logic generates BERT pattern to be transmitted in the payload of the ATM cell. This logic is same as raw BERT logic and provides all functionalities like PRBS, Static and user defined Patterns. Error insertion is also part of this logic
- ATM Header Generator – This logic constructs traffic cell header using user provided values for VPI, VCI, GFC etc. The transmitter calculates the HEC value across the entire ATM cell header and inserts the result in the appropriate header field
- Cell Traffic Generator – This logic constructs the 53-byte ATM cell using the ATM header generated by the ATM Header generator block and puts the BERT pattern stream in the 48-byte payload area
- Idle Cell Generator – This logic provides Idle cells to rate control logic. Idle cells have constant headers and payload
- Cell Rate Controller – This logic controls rate of total traffic (both traffic cells as well as idle cells). IDLE:TRAFFIC cell ratio is derived from user defined traffic rate
- Scrambler – The ATM cell payload (48 bytes) can be scrambled before mapping into the T1 E1 Frame. A self-synchronizing scrambler with the generator polynomial x^43 + 1, as described in Recommendation I.432.1
- T1 E1 Framer – Frames the ATM cells into a T1 or E1 bit stream using direct mapping as defined by ITU specifications. T1 uses timeslots 0-23 and E1 uses timeslots 1-15 and 17-31 to carry

Receive ATM Block Diagram

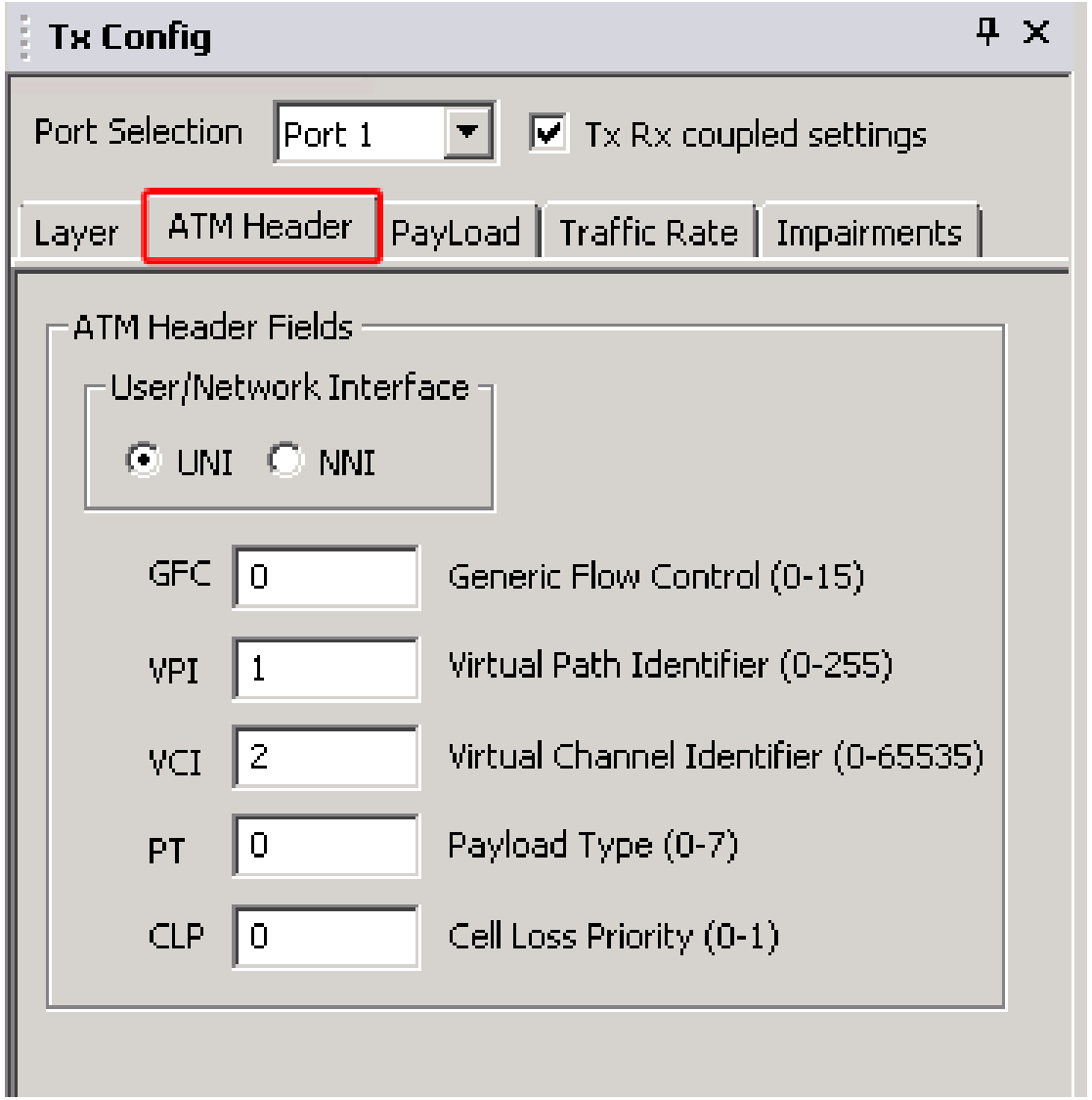


ATM Receive Description

- **T1 E1 Framer –** Gives raw data stream to the ATM block after removing the T1 or E1 framing information. ATM cells are carried over timeslots 0-23 for T1 and timeslots 1-15 and 17-31 for E1
- **ATM Cell Delineation and Descrambler –** This logic hunts for ATM cells by performing HEC calculation and keeps retrieving ATM cells while in sync mode. The ATM cell payload will be descrambled before being passed to the ATM layer
- **Idle Cell filter –** Filters out idle cells from the incoming cell stream
- **User Cell filter –** This logic filters desired cells based on user defined header information VPI, VCI, GFC etc. It checks the received header information like VPI, VCI, GFC etc. against the corresponding values set in the user defined header information. If the filter criteria matches then it extracts the payload and passes to the payload analyzer, otherwise it drops the cells
- **Receive Cell Statistics –** Determines the Cell statistics to be displayed by the application
- **BERT Verification –** This takes the payload data from the User Cell filter to determine pattern synchronization. This logic generates various BERT results

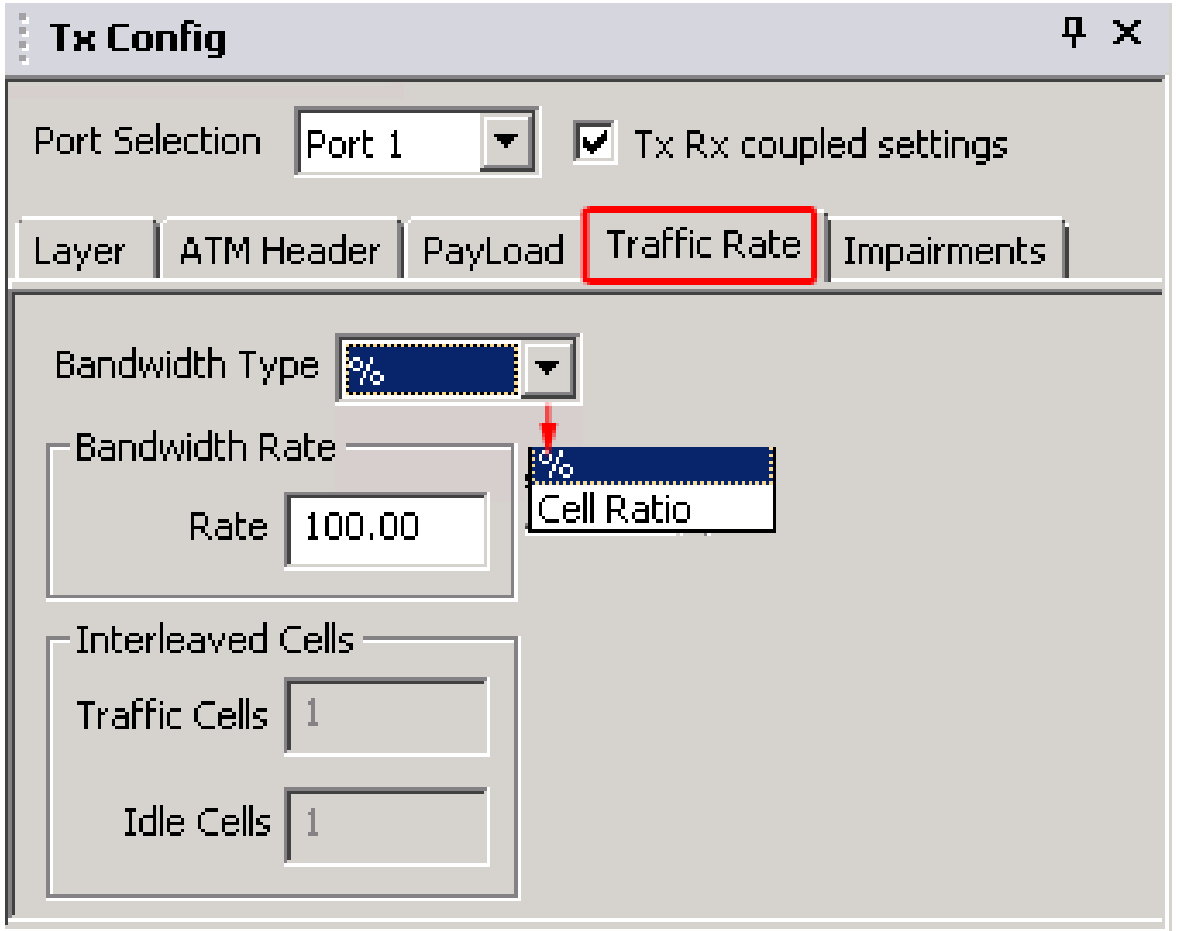
ATM Header Configuration

- Configures the ATM header fields such as VPI, VCI, PT, CLP, and GFC
- ATM header fields for UNI will have GFC (Generic Flow Control) enabled, while for NNI interface GFC field is disabled



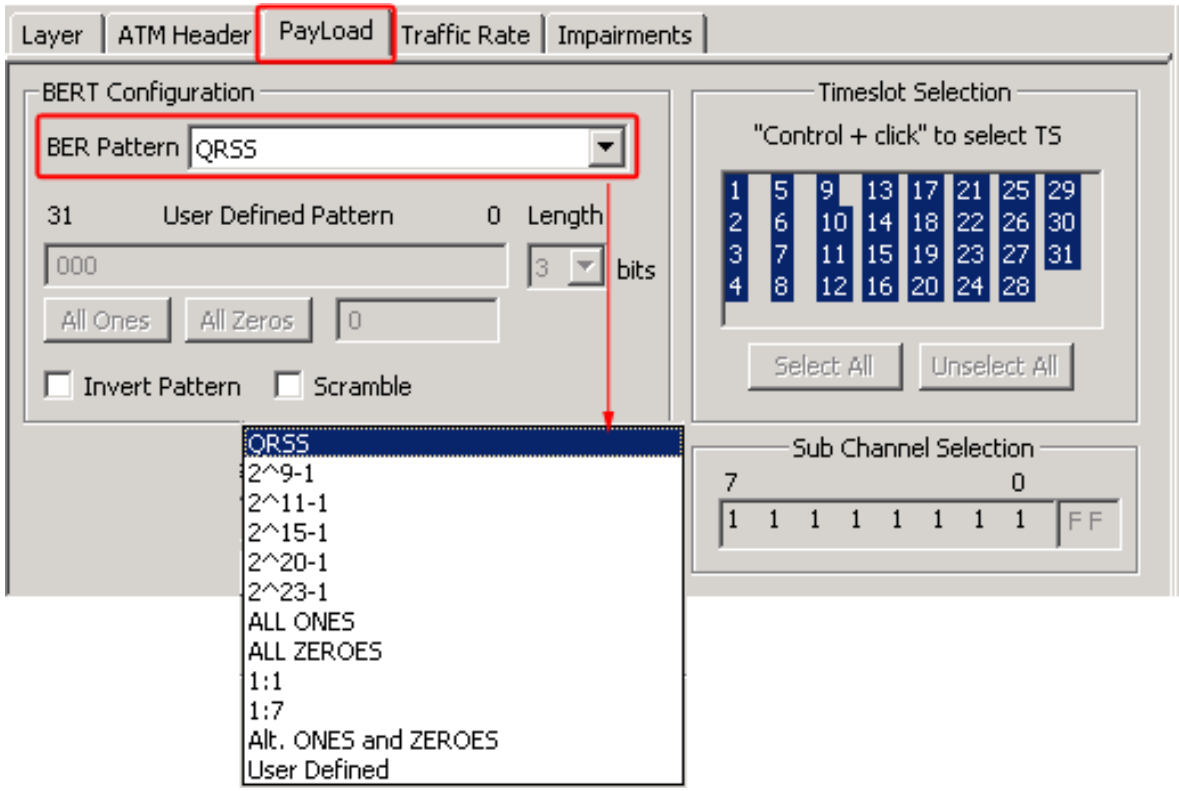
Traffic Rate

- The Traffic Rate for ATM BERT can be configured in two ways:
  - Percent of total bandwidth with range starting from 1% to 100%
  - Cell Ratio, where users can set the ratio of ATM traffic cells to idle cells



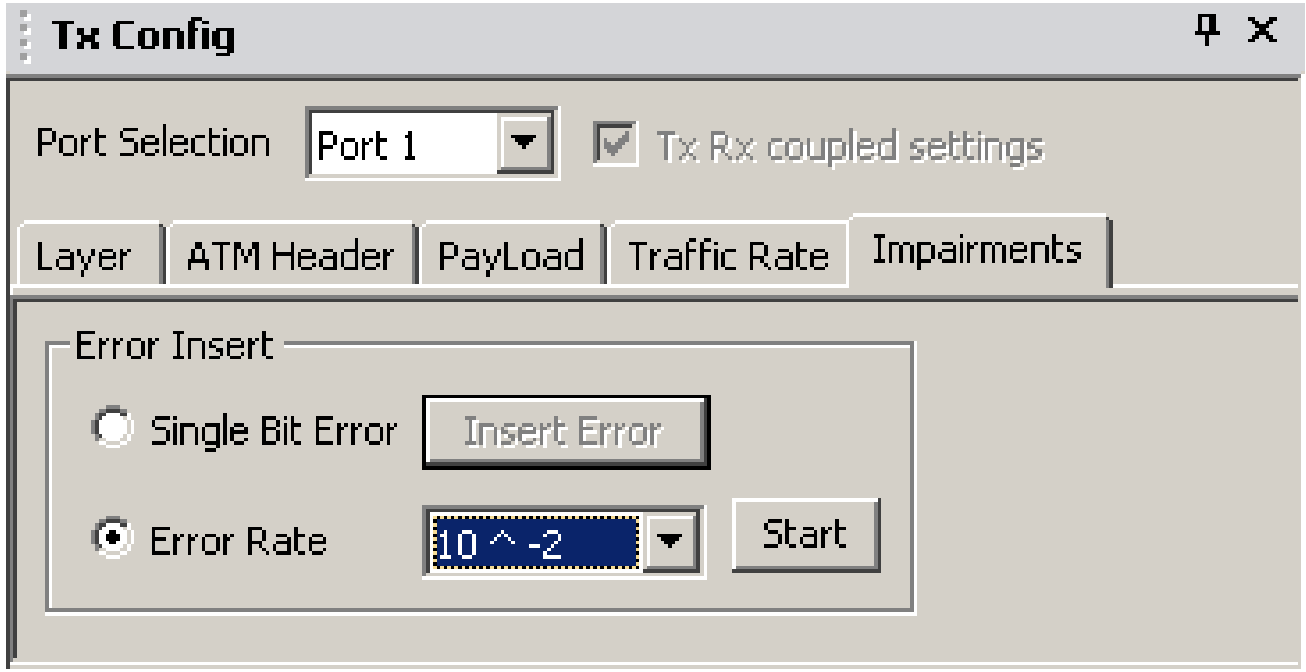
BERT Generation and Detection

- Payload at the Tx configuration allows user to select specific Bit Error Rate test pattern for transmission
- Supports various BERT patterns; QRSS, PRBS (2^9-1, 2^{11}-1, 2^{15}-1, 2^{20}-1, 2^{23}-1), fixed patterns like all ones, all zeros, alternate 1s and 0s, 1:1, 1:7, and user-defined patterns
- Rx configuration pattern is used to verify the incoming BERT pattern
- Other options such as invert and scrambling options (according to ITU-T G.804) are provided



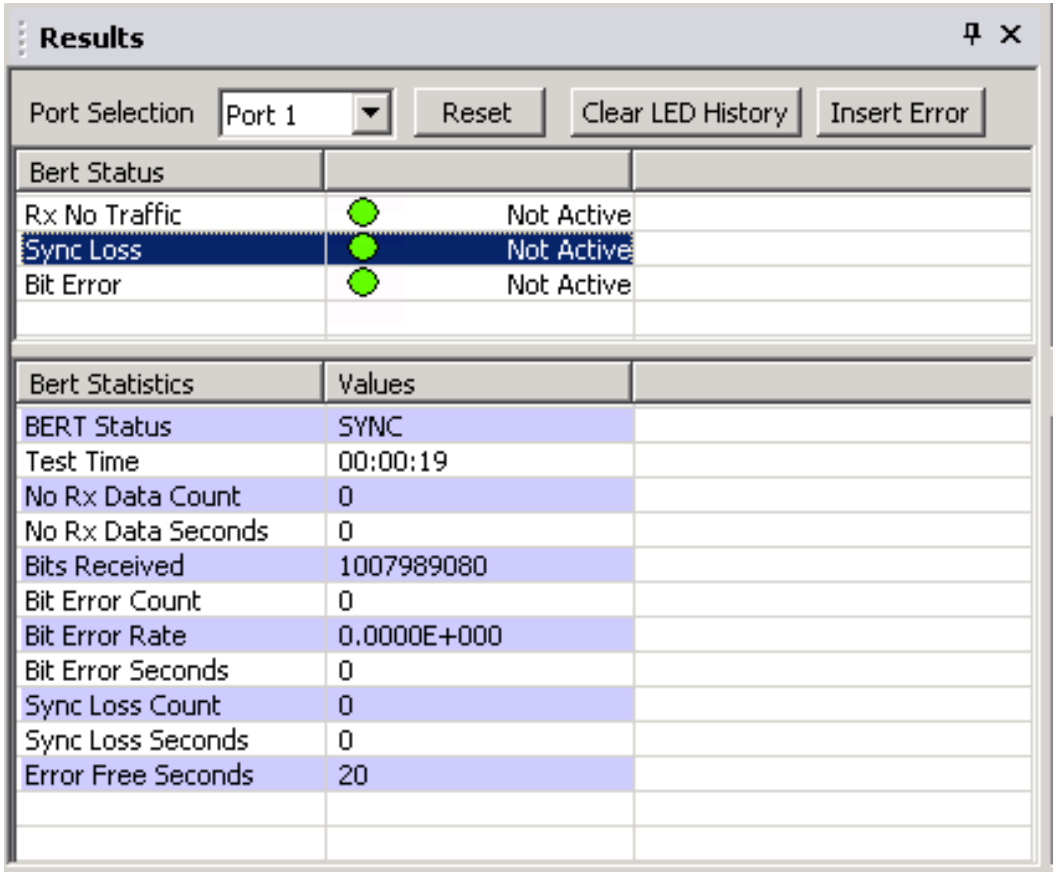
Error Insertion

- Allows single bit error insertion
- Also, supports Insertion of Error rate from 10^{-2} to 10^{-9} into the outgoing (TX) stream



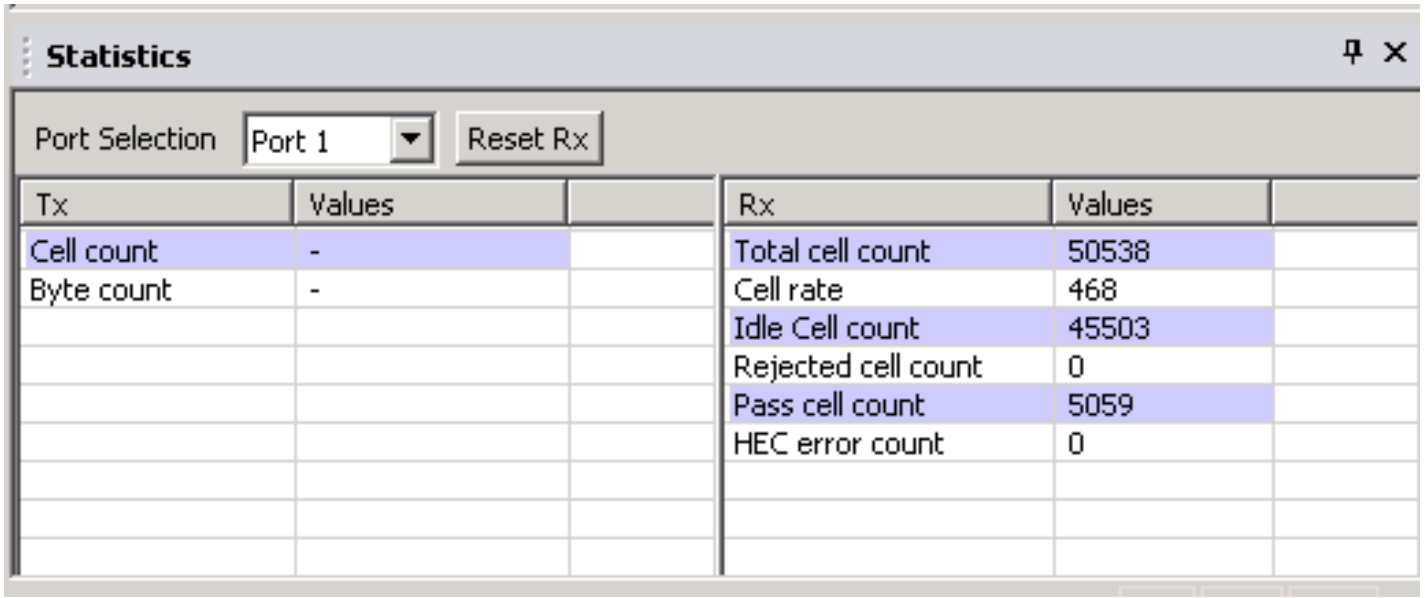
Results

- Displays both BERT Status with LEDs and BERT Statistics
- BERT statistics includes BERT status, Test Time, no Rx data, no Rx data seconds, bits received, bit errors, bit error rate, bit error count/seconds, sync loss count/seconds, and error free seconds
- BERT Status provides a quick view of the test status in the form of Alarm LEDs



Statistics

- Displays Tx and Rx statistics of the ATM BER test
- Rx statistics includes total cell count, cell rate, idle cell count, rejected cell count, pass cell count, and HEC error count



Thank you