USB Based T3 E3 Basic Applications



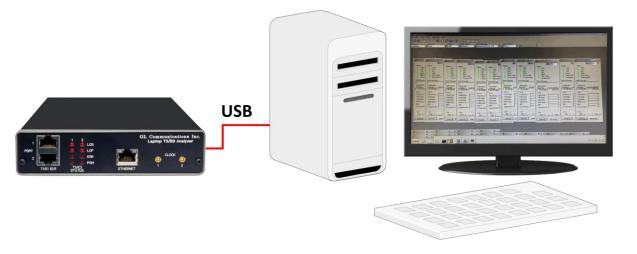
818 West Diamond Avenue - Third Floor, Gaithersburg, MD 20878 Phone: (301) 670-4784 Fax: (301) 670-9187 Email: <u>info@gl.com</u> Website: <u>https://www.gl.com</u>

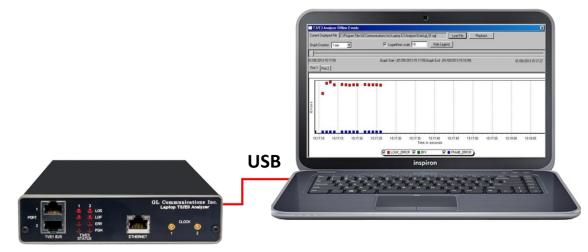
1

USB Based T3 E3 Analyzer

T3 E3 Analyzer unit can work with a Desktop or with a Laptop PC

- Lightest (1.75 pounds) unit available in the market
- Small footprint, easy to carry in the pouch of a Notebook PC - perfect for air travel
- Cost Effective
- Connects to a PC via a USB 2.0 port
- T3, E3, T1, E1, interfaces supported. Ethernet interface will be supported in future
- Remote access for controlling and monitoring will be provided in future







Front and Rear Views of the Analyzer

- Used for installation, test, and troubleshooting of T3 E3
 T1 E1 Ethernet lines
- Dual data stream capture capability
- Dropping and inserting T1 or E1
- Full Ethernet analysis
- HDLC, ATM, FR, and PPP analysis
- Used with GL's portable T1 E1 analyzer for individual T1, E1 analysis



Back Panel



Summary of Features & Benefits

- Software selectable T3 (DS3)/E3 interface along with T1 (DS1) and E1 Drop and Insert
- Dual T3 or E3 Receivers and Transmitters for non-intrusive and intrusive testing of both eastbound and westbound signals at the same time
- Simultaneously record/playback the entire T3 (DS3)/E3 in framed or unframed modes up to hard disk capacity
- Flexible clocking internal, recovered (from T3 (DS3)/E3, T1 (DS1) or E1) and external



Summary of Features & Benefits (Contd.)

- General T3 (DS3)/E3 signal testing capabilities
 - Alarms monitoring and logging
 - Monitor T3 (DS3)/E3 frequency, line level and various errors.
 - Alarm generation and error injection
 - Decode and simulate Far End Alarm Channel (FEAC) messages.
 - ➤ T3 (DS3)/E3 error counters
 - Dual BERT and G.821 Analysis
- Scripting and automation through GL's Windows Client Server (WCS) approach
- Monitor/manage the analyzer remotely via Ethernet port



Summary of Features & Benefits (Contd.)

- Channelized (Structured) Testing
 - Multiplex / De-multiplex T1 (DS1)/E1 signals (Drop and Insert)
 - Receivers for bidirectional monitoring with Dual T1 (DS1) / E1 drop
 - Transmit multiplexed externally inserted or internally generated T1 E1 streams into T3 (DS3)

/E3

- Stress test M13 (E13) multiplexers and 3/1 Digital cross connect systems
- > Dual channel drop and insert of T1 or E1 signals from any one of the T3(DS3)/E3 signals
- Broadcast or loopback individual T1s/E1s within the T3 (DS3)/E3
- Generates 28 T1s or (21 E1s) signals within the T3 (DS3) or 16 E1s within E3 output
- Unchannelized (Unstructured) Testing
 - > WAN Testing
 - Protocol testing for ATM, PPP, HDLC, and Frame Relay
 - Transmit / Verify HDLC frames with user defined headers



Basic Applications

- Bit Error Rate Test (BERT)
- Loopback Modes, Clock, Framing Formats, Structured/Unstructured Modes
- Transmit and Receive Configuration
- Monitor T1 or E1 Frames over T3 or E3 Lines
- Alarm Generation and Error Injection
- Tx Rx Memory Loopback
- Monitor Received Data
- Multiplex and De-multiplex T1 or E1 signals



Loopback Modes, Clock, Framing Formats, Structured/Unstructured Modes

E3 Interface Configuration Parameters

📕 Laptop E3 Analyze	r i								_ 🗆 🗵
Ele View Config M	onitor Applications Hel	þ							
📰 🎨 🎫	🔠 🇞 💥 🗖	🚺 🞑 🗒	J	HOLC Press PPP AT	M				
Rx Signal	Loopback	Framing		Clock Source	Mode Selection		Port Selection		
Terminate 💌	None	 Framed 	۳	Internal 💌	Unstructured	*	Port 1	2 🕿	
Terminate 💌	None	 Framed 	-	Internal 💌	Unstructured	*	Port 2	¥.	
Terminate	None	Framed		Internal	Structured (E3 to E	E1)			
Monitor	Outward Loopback	Unframed			Unstructured				
	Diagnostic Loopback			External					
				External (LS)					
				External LIU (T1)					
				External LIU (E1)					

T3 Interface Configuration Parameters

🔠 Laptop T3 Analyz	er	and an and a second			
Ele Yew Config M	Ionitor Applications Help				
Rx Signal	Loopback	Framing	Clock Source	Mode Selection	Port Selection
Terminate 💌	None	C-Bit 💌	Recovered	Unstructured	Port 1 💌 🔿
Terminate 💌	None	C-Bit 💌	Internal 💌	Unstructured 💌	Port 2
Terminate	None	M13	Internal	Structured (T3 to E1)	
Monitor	Outward Loopback	C-Bit	Recovered	Structured (T3 to T1)	
	Diagnostic Loopback	Unframed	External	Unstructured	
		,	External (LS)		
			External LIU (T1)		
			External LIU (E1)		



Transmit and Receive Configurations

Tx/Rx parameters for the T3 signal

🔢 Tx and Rx Configuration #1					
Transmit Configuration	Receive Configuration	Т	x/Rx parameters	s for the E3	signal
Frame Error Insertion Insert Four M-Bits Frequency Offset OFF OFF ON 850 Hz FEAC Messaging Binary DS3 AIS Received Xx010110 Channel Selection DS3 Line Burst Continuous	Frame Error Counting Count F & M Bits	Frame Error 1 Frequency OFF ON FEAC Mess DS3 Out of Channel Sele E3 Line FEAC me	Insertion Insert Four FAS Words Offset 309 Hz saging Binary Frame	Receive Configuration — Frame Error Counting Cou	Int Bit Errors(FAS)
Use self test to verify the unit's internal function on self test means that the unit is working prope			test to verify the unit's internal functio est means that the unit is working prop C		Self Test



Transmit and Receive Configurations (Contd.)

- Possible frame error insertions in T3
 - ➢ Single FAS word (1111)
 - ➤ Single FAS word (0000)
 - Four FAS words (1100)
 - Four FAS words (0011)
- Possible frame error insertions in T3
 - ➢ Single F Bits
 - ➤ Single M Bits
 - ➢ Four F Bits
 - ➢ Four M Bits
- Frequency Offset ranging from +50 to -50 ppm for the internal clock source
- Standard and User-defined FEAC Message transmission (only for T3 Systems with C-Bit Parity Framing Format)
- Frame Error Counting
 - E3 Bit Errors (FAS), Word Errors (FAS)
 - ➤ T3 F & M Bits , F Bits , M Bits
- Self Test the unit



Transmit and Receive Configurations (Contd.)

FEAC Message (only for T3 Systems with C-Bit Parity Farming Format)

- Using the FEAC channel, alarm or status information from the far-end terminal can be sent back to the near-end terminal
- The Monitor T3 Line indicates the incoming FEAC message

🔚 Tx and Rx Configuration #1		Monitor #1
Tx and Rx Configuration #1 Transmit Configuration Frame Error Insertion Frequency Offset OFF OFF OFF	-Receive Configu Frame Error Cour	Monitor #1
 ON 850 Hz ▼ FEAC Messaging Binary D53 AIS Received × xx010110 Channel Selection D53 Line ■ Burst Continuous 		FEAC Message DS3 AIS Received Signal input Freq (Hz) Level (Vp) 44736000 1.40 Errors Frame Errors 0 P-Bit Parity 0 C-Bit Parity 0 FEBE Errors 0 BPV 0
Use self test to verify the unit's internal function on self test means that the unit is working prope C		Excessive O's 0



Alarm & Error Display for T3 (DS3) & E3

T3 Monitoring	E3 Monitoring
Monitor #2	Monitor #1
Alarms Alarms IOS IOF AIS IDLE RAI / X-BIT Excessive 0's FEAC Message Signal Input Freq (Hz) Level (Vp) 44736000 1.22 Errors Frame Errors S P-Bit Parity Q FEBE Errors 1 BPV 2 Excessive 0's 0	Alarms LOS LOF Als Als RAI / X-BIT Excessive 0's FEAC Message Signal Input Freq (Hz) Level (Vp) 34368000 1.69 Errors Frame Errors O CV 0 Excessive 0's 0
🗖 Log Alarms	🔽 Log Alarms
Reset All Hide Panel	Reset All Hide Panel



Alarm and Error Display for T3 (DS3)

- Available alarms are
 - LOS (Loss of Signal)
 - LOF (Loss of Frames)
 - ➤ AIS (Alarm Indication Signal)

≻ Idle

- ≻ RAI/X-Bit
- Excessive 0's
- Error Indications

➤ Frame

➢ P- Bit parity

➤ C-Bit parity

➤ FEBE

➢ BPV

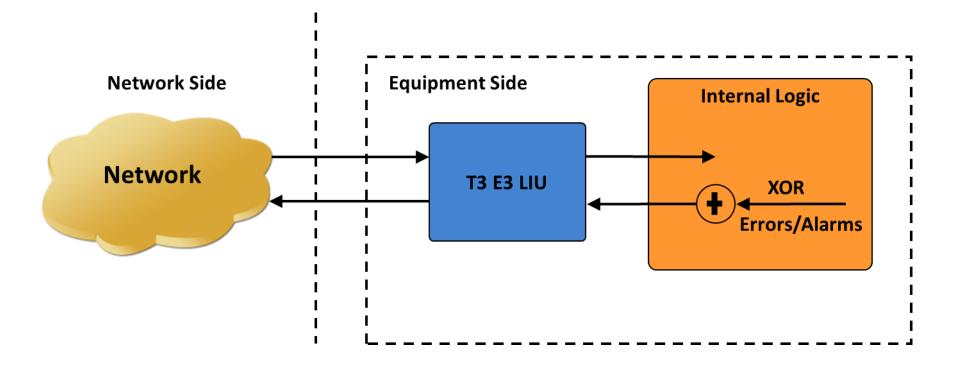
≻ CV

Excessive zeros

Image: Signal Incomposition Point Point <t< th=""><th>Ele View Config Monitor Applicatio</th><th>ns Heln</th><th></th><th></th><th></th><th></th><th></th><th><u>X</u></th></t<>	Ele View Config Monitor Applicatio	ns Heln						<u>X</u>
Rx Signal Loopback. Framing Obck. Source Mode Selection Port Selection Terminate None C-Bit Internal Unstructured Port Context Terminate None C-Bit Internal Unstructured Port Context Terminate None C-Bit Internal Unstructured Port Context Context Terminate None C-Bit Internal Unstructured Port Context Context Terminate None Context Terminate None Port Context Context Terminate None Context Terminate None Port <	7			HDLC Frame F	PPP A1	M	 	
Terminate None CBit Internal Unstructured Port 2 Image: Construct of the state of the stat	Rx Signal Loopback		Framing	Clock Source		Mode Selection		
Monitor #1 Port #1 Port #1 Port #2 Alams LOF Alams DIDLE Pal/XBIT Excessive 0's FEAC Message Image: Signal Input Freq Hz1 Level Vp (dBdsx) Freq Hz2 Level Vp (dBdsx) Frame Enors Frame Enors Frame Enors Frame Enors Frame Enors Party BPV C-Br Parity C-Br Parity D BPV Cog Start Stort Start			100 million (100 m					
Alams I LOS I LOF I Alams I LOF I Alams I LOF I Alams I LOF I Alams I LOF I Alams I LOF I Alams I LOF I Alams I LOF I Alams I LOF I Alams I LOF I Alams I LOF I Alams I DLE I RAI /X-BIT I Excessive 0's I Log I RAI /X-BIT I Excessive 0's I Core I Signal Input Frame Errors I Pait Parity I Core I Core I Signal Input Frame Errors I Pait Parity I Pait Parity I Pait Parity I DE I Excessive 0's I De I Log <	l erminate None		L-Bit	Internal		Unstructured	Port 2	
Alarms Alarms I LOS LOS Alarms LOS BAlary DIDL BAlary DIDL Frequestrant Frequestrant Frame Errors D Frame Errors D BPV D BPV D BPV D BPV D Bread Hyb D Excessive 0's D BPV D </th <th>Monitor #1</th> <th>× 🖪</th> <th>Monitor #2</th> <th></th> <th></th> <th></th> <th></th> <th></th>	Monitor #1	× 🖪	Monitor #2					
LOS LOS LOF L	Port #1		J P	ort #2 💌				
For Help, press F1	LOS LOS LOF AlS IDLE RAI / X-BIT Excessive 0's FEAC Message Signal Input Freq (Hz) Level Vp (dBdsx) 44 736 000 0.78 (0.9) Errors Frame Errors O P-Bit Parity O C-Bit Parity O Excessive 0's O BPV O Excessive 0's O Log Start Stop View		LOS LOF AIS IDLE RAI /X-BIT Excessive 0 FEAC Message Signal Input Freq (H2) Leve 44 736 000 Errors Frame Errors P-Bit Parity C-Bit Parity FEBE Errors BPV Excessive 0's Log Start Stop	el Vp (dBdsx) 0.87 (1.9) 0 0 0 0 0 0 0 0 0 0 0 0				



Alarm Generation and Error Injection



- Internally generates various types of errors and / or alarms and transmits them on the outgoing T3 (DS3)/E3 stream
- Automatically inserts single bit errors or at regular intervals of time (secs)



Alarm Generation and Error Injection (Contd.)

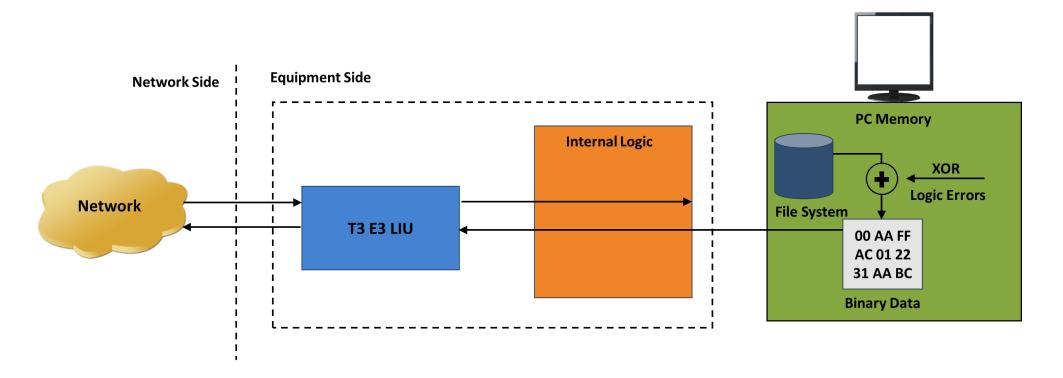
📲 Alarm And Error Generation #1	🔚 Alarm And Error Generation #1 📃 🗆 🗙
E3 Errors Single Cont. Frame Errors 1 1 CV 1 1 Excessive 0's 1 1 Error Rate 10^-3 User Defined Rate 1.00E-002 Close	T3 Errors Single Cont. Frame Errors P-Bit Parity C-Bit Parity I C-Bit Parity I FEBE Errors BPV I Excessive 0's I Error Rate I0^-3 User Defined Rate 1.00E-002 Close

- Alarms LOS (Loss of Signal), LOF (Loss of Frames), AIS (Alarm Indication Signal), Idle, RAI/X-Bit, Remote Alarm Indication (RAI)
- Errors Frame, P-Bit Error (T3 Only), C-Bit Error (T3 Only), FEBE Error (Far End Block Errors) (T3 Only), BPV BiPolar Violation (T3 Only), Excessive 0's, CV Errors (E3 Only)



Tx Rx Memory Loopback

Logical Diagram for Transmit and Receive Memory Loopback for T3 (DS3)/E3 Analyzers



- With the loopback, the data received from the network is retransmitted back via the PC memory
- Optionally logic errors (XOR) can be inserted into the loopback stream during loopback
- Allows insertion of single bit errors manually



Tx Rx Memory Loopback (Contd.)

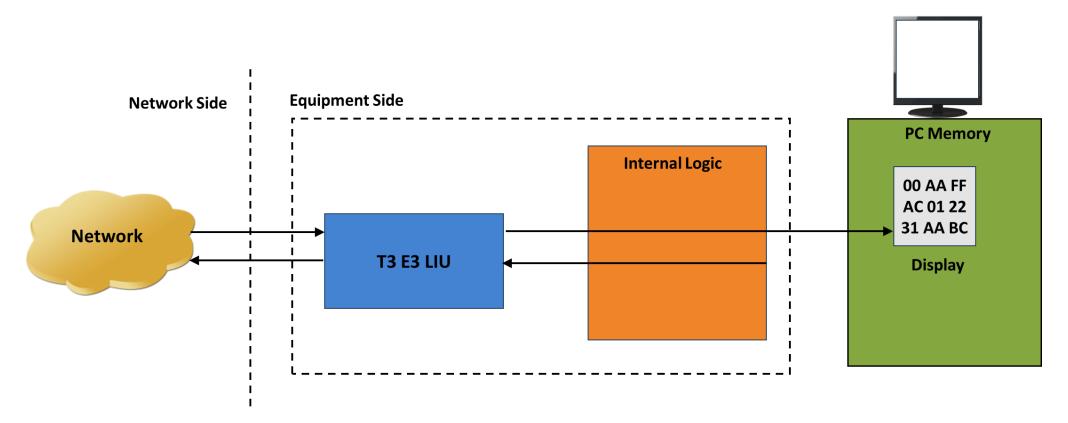
🔚 Rx To Tx In-memory Loo	pback			_ 🗆 🗙
Select a "Source" port and "Destination" port and then the Start button.	a	Source (Rx) #1 #2	Destination #1 #2	(Tx)
Performance and Results	igle Error	Close	Stop	
Item Description	Port #1 t	o #2		
Overruns (Underruns) Missed Xfers - Rx (Tx) Skipped Bytes - Rx (Tx) Skipped Blocks - Rx (Tx)		0 #2 5 (28260615)		

- Used for diagnostic purposes
- Memory Loopback and Bit Error Rate Test applications can be run on two different ports simultaneously to verify the operation of the analyzer unit



Monitor Received Data

Logical diagram for the Monitor Received Data application



• This application can monitor raw bit values on the selected ports. The raw bytes received from the network at the T3 interface are monitored and displayed on the selected ports



Monitor Received Data (Contd.)

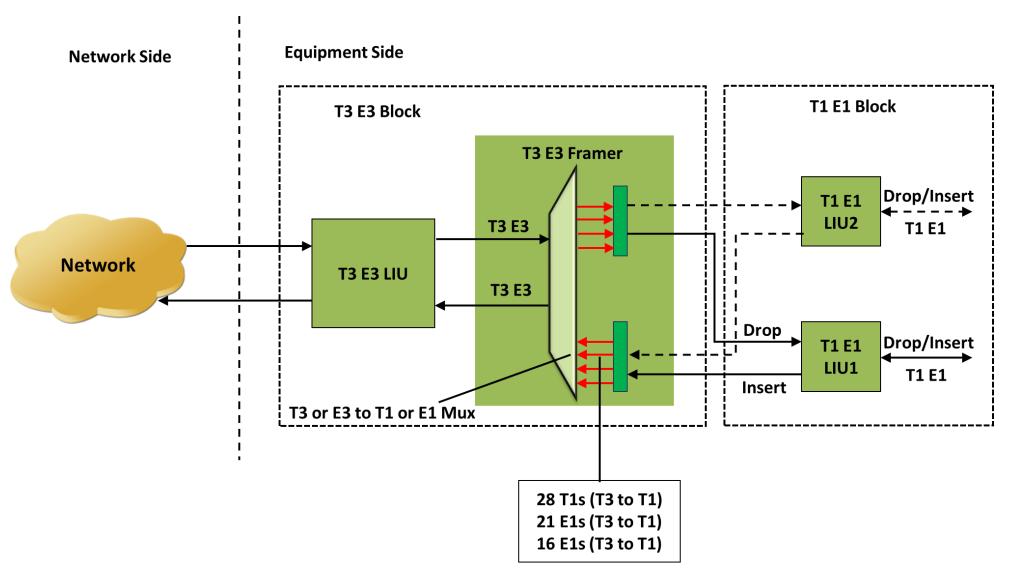
Performance and Results Item Description Port #1	_ 🗆
Performance and Results Item Description Port #1	ction —
Overruns 0	
Missed Xfers 0	
Skipped Bytes 0 Skipped Blocks 0	

- Used for quickly testing the byte alignment of the received data
- Underruns, MissedXfer, Skipped Bytes, and Skipped Blocks display provides the receive data pipe performance



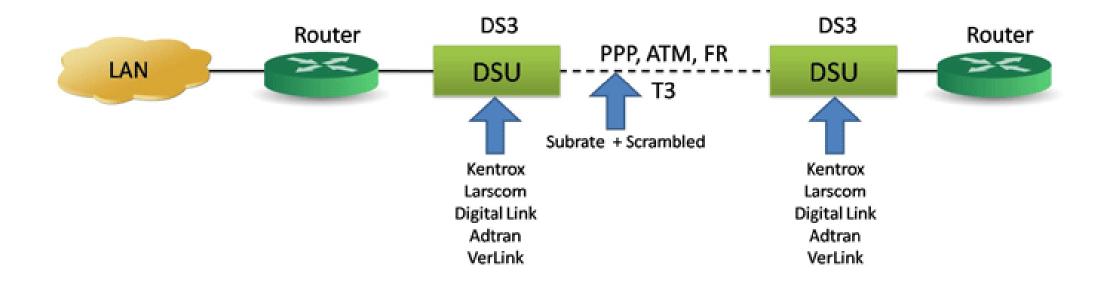
Multiplex and De-multiplex T1 or E1 signals

Logical Diagram for Drop and Insert Structured Mode



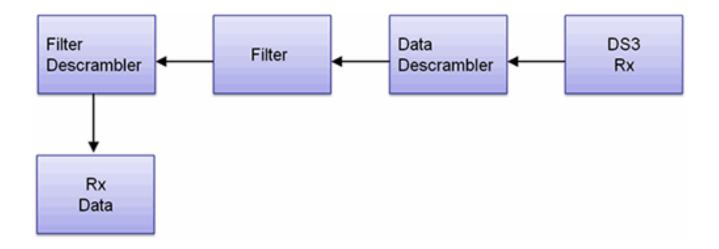


T3 (DS3) Subrate and Scrambling





DS3 Subrate Block Diagram





Auto Config

DSU Subrat	e Config	×
Ports DSU Type Rx DS-3 Bai	Digitallink 💌	Apply to all Ports
300000K	3900000K	7500000K
600000K	4200000K	7800000K
900000K	4500000K	8100000K
1200000K	4800000K	8400000K
1500000K	5100000K	8700000K
1800000K	5400000K	9000000K
2100000K	5700000K	9300000K
2400000K	6000000K	9600000K
2700000K	6300000K	9900000K
3000000K	6600000K	1020000K
3300000K	6900000K	1050000K
3600000K	7200000K	10800000K
Auto	Config	Þ
Trying P	ort#1, Adtran, 4413000	00 Abort



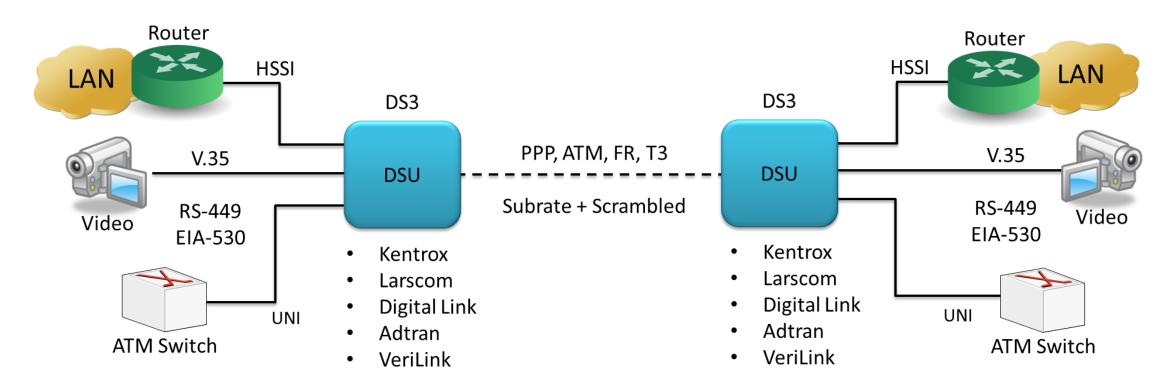
DS3 Subrate Configuration Setup

11	T3 Analyzer						_ 7 ×
	Config Monitor Applications Help						
	BER 1995 🎇 🖾 🔝 🞑						
Px Signal Terminate	Loopback None	Framing C-Bit	Clock Source	Mode Selection	•	Port Selection	
Terminate	None			■]Onstructured	<u></u>	1-00.1	
	Monitor #1						
	Alarms		DSU SU	brate Config	×	1	
	C LOS					1	
	 LOF AIS 		Pol	rts #1			
	IDLE		DSU TY	Adtran	Enable Scrambling		
	 RAL/X-BIT Excessive 0's 		-2.4440071174		∏ Rx		
E	EACMessage		Rx DS-3	Bandwidth			
	-		80K 150K	1280K	2480K		
	Signal Input		230K	1350K	2560K 2630K		
Let the second se	Freq (Hz) Level Vp (dBdsx) 44 736 096 0.76 (0.7)		300K 380K	1500K	2710K 2780K		
	Errors		450K 530K	1650K	2860K 2930K		
1200	Frame Errors 0		600K 680K	1800K 1880K	3010K 3080K		
F	P-Bit Parity 0		750K	1950K	3160K		
	C-Bit Parity 0 TEBE Errors 0		900K	2030K 2110K	3230K 3310K		
1923	EBE Errors 0		980K 1050K	2180K 2260K	3380K 3460K		
	Excessive 0's 0		1130K 1200K	2330K 2410K	3530K 3610K		
			1200K	2410K	3010K		
- L	-og					J	
	Start Stop View						
	Reset All Hide Panel						

 The user has the ability with the USB T3 E3 unit to configure the DSU and the rate using the DS3 Subrate Config window as shown in the screen capture



Scrambling and Subrate



- For Data, Packetized Voice, and Video and other Unchannelized Uses
- Generally, not for 28 T1s



DSU Types

o Sabrace	Config	
Ports	#1 💌	
DSU Type 🚦	Digitallink 🗾	Enable Scrambling
		🔽 Rx
tx DS-3 Band	haidth	
300K	4800K	9300K
600K	5100K	9600K
900K	5400K	9900K
1200K	5700K	10200K
1500K	6000K	10500K
1800K	6300K	10800K
2100K	6600K	11100K
2400K	6900K	11400K
2700K	7200K	11700K
	7500K	12000K
3000K		100001/
3000K 3300K	7800K	12300K
	7800K 8100K	12300K 12600K
3300K		
3300K 3600K	8100K	12600K

Larscom Subrate DSU Subrate Config × • Ports #1 -Enable Scrambling -DSU Type Larscom 🔽 Rx Rx DS-3 Bandwidth 3200K 6300K 9500K 12600K 15800K 18900K 22100K 25300K 28400K 31600K 34700K 37900K 41100K 44210K

Verlink Subrate

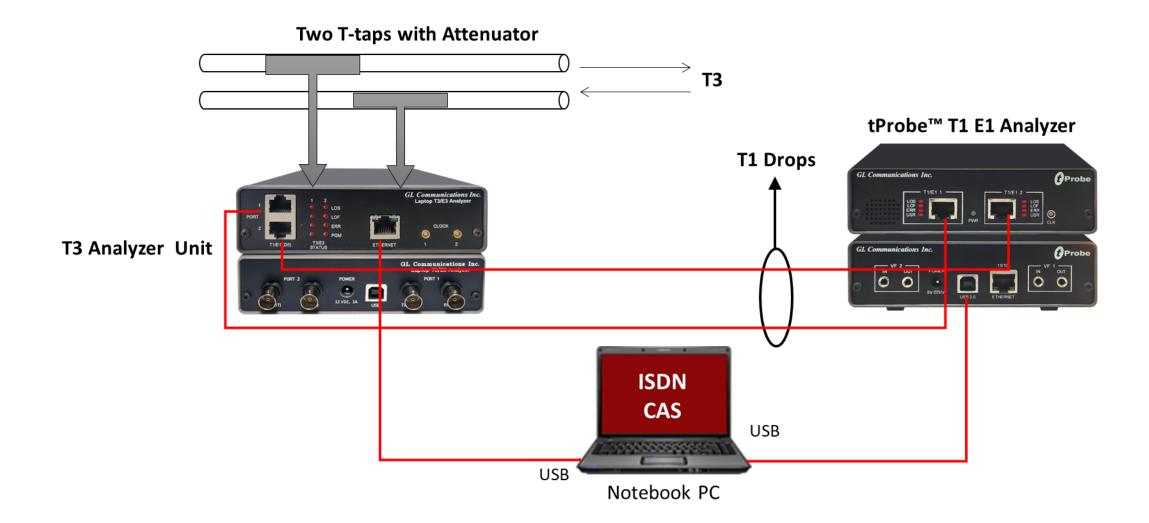
5U Subrat		2
Ports	#1	
DSU Type	Verilink	Enable Scrambling -
Rx DS-3 Bar	ndwidth	<u>.</u>
1600K	25300K	
3200K	26800K	
4700K	28400K	
6300K	30000K	
7900K	31600K	
9500K		
11100K		
12600K		
14200K		
15800K		
17400K		
18900K		
20500K		
22100K		
23700K		

Adtran Subrate

Ports	#1 •	
DSU Type 🛛	Adtran 🔽	Enable Scrambling
₹x DS-3 Band	lwidth	
80K	1200K	2330K
150K	1280K	2410K
230K	1350K	2480K
300K	1430K	2560K
380K	1500K	2630K
450K	1580K	2710K
530K	1650K	2780K
600K	1730K	2860K
680K	1800K	2930K
750K	1880K	3010K
830K	1950K	3080K
900K	2030K	3160K
980K	2110K	3230K
1050K	2180K	3310K
1130K	2260K	3380K



T3-T1





Multiplex and De-multiplex T1 E1 Signals

User interface for the Structured Mode (Drop / Insert) Settings

Tx Settings					Port #1
1	Loopback 3	AIS	Insert #1 🔶	Insert #2 🖛	Ě
					k.
1 🔁1	2 격1 3	(1] 4 (5 🔁	6 🔁 7 🔁	8 👧
9 📶	10 쓀 1	1 21 12 0	B 13 (2)	14 🧔 2 15 👧	16 👧
17 🦕	18 뛸 19	9 🛐 _ 20 🛔	21 🦕1	22 격1 23 👧	24 (115
25 📶	26 윌 2	7 🗃 28 🕯		Apply To All Ch	annels
Drop Port Settin	gs Channel Selectio	orop Port #1 (T1)	Drop Port #2	(T1)	

- Up to two user selected T1 (or E1) channels can be externally inserted using the T1 E1 input/output interface into any one of the transmitted T3 (DS3) or E3 signal
- The inserted T1 or E1 signal can be selectively transmitted through one or more of the T1 E1 transmit channels or broadcasted through all the T1 E1 channels
- Up to two user selected T1 or E1 channels can be dropped



Bit Error Rate Test - BERT (Full Frame & Unframed)

(FT)	USB T3 Analyzer
<u>F</u> ile <u>V</u> iew Config N	Aonitor Applications <u>H</u> elp
Bert	Enhanced BERT Untitled
File Actions View	Windows Help
🚬 🔳 🗸 🗙 💡	
Port #1	Ber Tx Rx Settings - Port #2
	IN Settings [Testal] Image: Transmit Receive Coupled Settings (Tx=Rx) Apply To All Ports Image: BER Patterns Image: Transmit Receive Coupled Settings (Tx=Rx) Image: BER Patterns Image: Transmit Receive Coupled Settings (Tx=Rx) Image: BER Patterns Image: Transmit Receive Coupled Settings (Tx=Rx) Image: BER Patterns Image: Transmit Receive Coupled Settings (Tx=Rx) Image: BER Patterns Image: Transmit Receive Coupled Settings (Tx=Rx) Image: BER Patterns Image: Transmit Receive Coupled Settings (Tx=Rx) Image: BER Patterns Image: Transmit Receive Coupled Settings (Tx=Rx) Image: BER Patterns Image: Transmit Receive Coupled Settings (Tx=Rx) Image: All Zeros Image: Transmit Receive Coupled Settings (Tx=Rx) Image: All Zeros Image: Transmit Receive Coupled Settings (Tx=Rx) Image: All Zeros Image: Transmit Receive Coupled Settings (Tx=Rx) Image: All Zeros Image: Transmit Receive Couple Settings (Tx=Rx) Image: All Zeros Image: Transmit Receive Couple Settings (Tx=Rx) Image: All Zeros Image: Transmit Receive Couple Settings (Tx=Rx)
	All Rits Inverted Length 32 -
	Graph - Online Display
	○ I Real-Time Display Graph Duration 10 sec ▼ Clear Hide Legend Print
	03/17/2016-12:53:01 Graph Start - (03/17/2016-14:19:40) Graph End - (03/17/2016-14:19:50) 03/17/2016-14:19:50 Port 1 Port 2
	ygu 14:19:40 14:19:41 14:19:43 14:19:45 14:19:45 14:19:46 14:19:47 14:19:48 14:19:49 Time in seconds Image:
Start Stop	

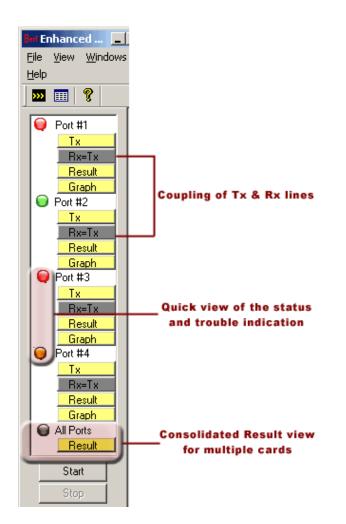
• GL's T3 E3 Bit Error Rate Tester application measures the correctness of data received on T3 E3 channels for a repetitive fixed or pseudorandom pattern for the given transmission



Selection of Port – View Error Status, Results

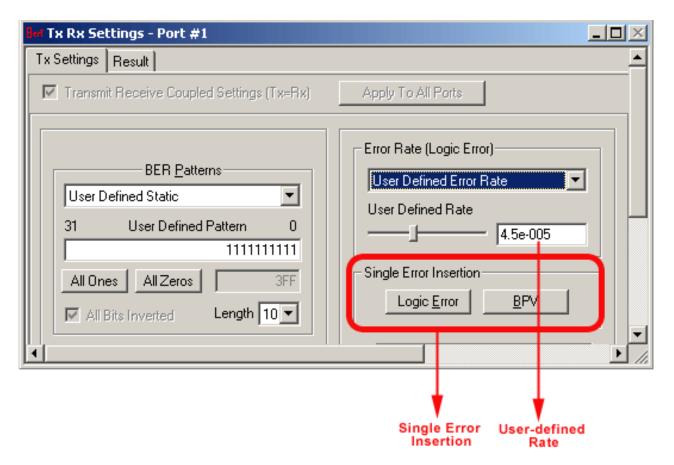
Bit Error Rate Test - BERT

- Quick view of the status and trouble indication
- Supports testing on multiple ports simultaneously with consolidated result view
- Tx and Rx settings for multiple ports can be independently controlled or they can be coupled (Apply to All) from a single card to all cards





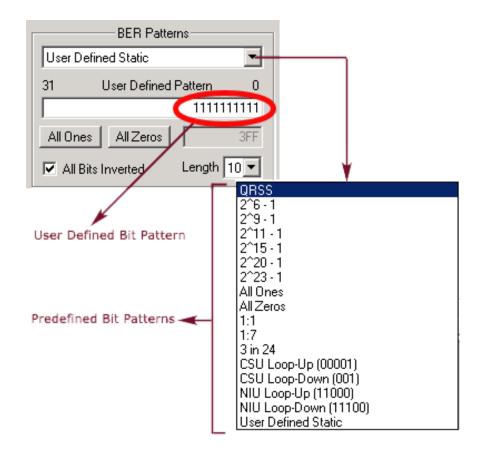
Error and Bit Patterns Insertion



- Supports pre-defined and user defined error insertion rate ranging from 10^-2 to 10^-9 (0.01 to 1e-009)
- Automatic insertion of Logic and BPV errors at regular intervals of time (secs) or just insert single bit errors into the transmit stream



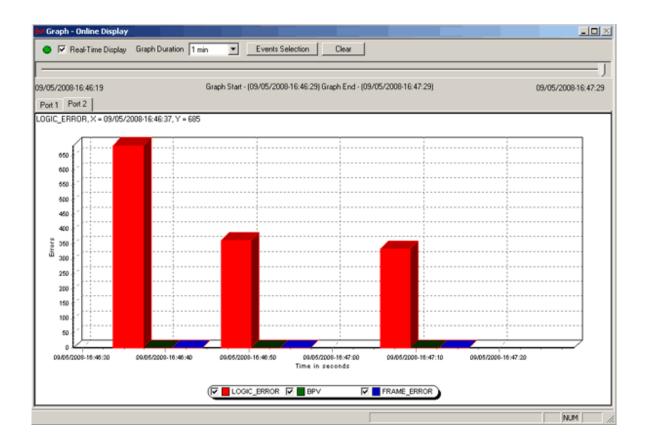
Static and User-Defined Pattern Selection



- Generates standard static bit patterns such as QRSS, 2^5-1, All ones, All zeros, 1:1, CSU Loop-Up (0001), CSU Loop-down (001), NIU Loop-UP (11000), NIU Loop-Down (11100), and more
- Generates user-defined static patterns of size up to 32 bits



Graphical Result



- The Error Count Vs Time graph of the bit error test results is displayed
- For real-time graph, the predefined or the user defined bit pattern and the errors can be inserted
- Offline graph display the saved (*.xml) files are loaded for analysis
- Any of the events such as LOGIC_ERROR, BPV, or FRAME_ERROR can be set for the display



Thank you

