LightSpeed1000[™](w/ GigE and USB 2.0) (Legacy Product)

(OC-3/STM-1, OC-12/STM-4 Analysis and Emulation Card)



Overview

GL's LightSpeed1000[™] hardware platform (available as PCIe Card and USB Pod) is capable of OC-3/12 and STM-1/4 wirespeed processing on quad optical ports for functions such as wirespeed recording and wirespeed playback of Unchannelized and Channelized ATM, PoS, RAW Traffic. Two ports out of the 4 ports are meant for SONET/SDH unchannelized and unframed data. The remaining two ports are meant for SONET/SDH channelized data of carrying many independent unframed/framed T1, E1, T3, and E3 streams

The LightSpeed1000[™] comes with software for overall monitoring, BERT, emulation, and protocol analysis with a price tag that compares very favorably with similar test instruments at three times the price. In an OC-3/STM-1, all 84 T1s or all 63 E1s can be identified and processed in transmit and receive modes. In an OC-12/STM-4, all 336 T1s or all 252 E1s can be identified and processed in transmit and receive modes.

The hardware can also be easily configured / programmed for delaying of ATM Cells or PPP packets. The card's multiple connectivity using PCIe, Gigabit Ethernet (GigE), USB 2.0, and onboard DDR2 memory makes it suitable for various applications.

For more details, refer <u>LightSpeed1000™</u> webpage.

Main Features

Hardware ED-137 Signaling Simulation

- *Multiple cards per system for super high capacity monitoring and test system
- High performance x4 PCIe interface with optimized DMA to perform Rx and Tx packets to/from PC memory
- Hardware based precise time-stamping of cells with 10 nsec resolution, 1 ppm accuracy

Analyzer Features

- Software selectable OC-3 / OC-12, or STM-1 / STM-4 for Unchannelized ATM, PoS or Transparent Traffic, and Channelized T1, E1, T3, E3 traffic
- API Toolkit to develop user specific applications



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Main Features (Contd.)

Traffic

- *Wirespeed processing of ATM, PoS or RAW data for Tx and Rx for both ports
- *Precisely emulates packet delays that occur over SONET/SDH carrying ATM or PoS traffic, delay is adjustable from 1 ms to maximum of 500 msec
- Ability to capture/playback to/from disk at full rate in both directions for all ports for detailed offline analysis
- Simultaneous synchronous capture or transmit is possible on all optical ports
- Comprehensive transmit/receive testing capabilities; transmitting and verifying data with incrementing sequence numbers with each packet/cell

BERT

• Easy to use and flexible Bit Error Rate Test (BERT) application for ATM, POS, and RAW

Protocol Testing

• ATM (AAL2, AAL5) Protocol Analyzer, UMTS Protocol Analyzer, PPP (IP and higher layer protocols) Protocol Analyzer

*PCIe card only

PoS Analyzer– Packet Over SONET / SDH

Overview

PoS, or Packet over SONET / SDH—OC-3/STM-1 and OC-12/STM-4 is supported at full rates over. Access, capture, analysis, and emulation of PPP and HDLC, all carrying IP traffic in real-time makes this card useful to many applications including routing, deep packet inspection, and other internet traffic applications.

PoS Protocol Analysis

PPP Analyzer can be used to capture a host of PPP protocols exchanged between the two nodes over SONET/SDH link. User can obtain detailed analysis of higher later protocols (IP, TCP, UDP, HTTP, FTP, POP3 etc.) and can perform various statistics measurements. Integrated Packet Data Analysis (PDA) in Real-time PPP Analyzer is an outstanding tool for live monitoring of VoIP traffic. It can segregate IP traffic into SIP / H323 / MEGACO / MGCP calls and collects statistics, CDRs, ladder diagrams, and a host of other useful information about VoIP calls.

PPPP Pr	otoco	ol Analy	sis Pl	PP .																						
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$\sqrt{2}$	0	((0.00.00	0.0000	00000	10	030		l In	sternel	Protocol	1	192.1	68.1.1	111	15	92.168	1.222		2	0001			10001	
V 2	0	1	1	0:00:00	0.000	13770	10	030		In	ternet	Protocol	1	192.1	68.1.1	111	19	32.168	1.222	2	21	0001			10001	
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00 21 4 01 6F 0 00 00 0 00 00 0 00 00 0	45 0 C0 A 00 5 00 5 00 5	0 03 8 01 A 67 A 67 A 67 A 67 A 67	FD 1 DE 4 CF 0 CF 0 CF 0 CF 0	2 34 E 21 0 00 0 00 0 00 0 00	00 27 00 00 00 00	00 F 11 0 00 0 00 0 00 0	F 11 5 C8 0 5A 0 5A 0 5A 0 5A	48 FA 67 67 67 67	OF 16 CF CF CF CF	A 00 0 00 0 00 0 00 0 00	8 0 0 0 0 0	IE OÀ	ZgI ZgI ZgI ZgI ZgI	4 NI'	ÿ H Êú Zg Zg Zg Zg	Å I I I										
Off-line Vie	wing							C	Docum	ents a	nd Sel	tings\Sa	meer	De 47	2079 F	ram	es	_	_				*****			-

Figure: PPP Protocol Analyzer

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PoS Port Configuration

PoS Port Configuration allows users to select FCS type, control FCS stripping on Rx and FCS appending on Tx.

POS Port Configuration				×
Attribute	Port 1	Port 2		
Rx FCS Bit Count	32 bits	32 bits		
Rx FCS Octets Present Tx Append FCS	strip 32 bits	strip 32 bits		
Port 1 32 b Port 2 16 b none	its e			
			Modify Defau	ılt Exit

Figure: PoS Port Configuration

PoS BERT

Support for the following PRBS Patterns: $2^9 - 1$, $2^{11} - 1$, $2^{15} - 1$, $2^{20} - 1$, $2^{23} - 1$, $2^{29} - 1$, $2^{31} - 1$, all one's, all zero's, alternate ones and zeros, user-defined pattern of lengths from 2 to 32 bits, invert and non-invert selections, single bit error insertion, error insert rate from 10^-1 to 10^-9, status for pattern sync, bit errors counters, and packet rate and packet gap configuration options, configurable header lengths and header information.

Pos Bert - [Untitled]								- 8 ×
Por File View Windows Help								_ 8 X
Ports: Port	1 •							
Configurations	Ty Config		Φx	· Py Config				ФX
Port 1	TA COMING			; Ka coning				
🖻 🤟 Bert - Tx	Port Selection Port 1	🔻 🗹 Tx Rx coupled set	tings	Port Selection Port 2 V	Tx Rx coupled settings			
Tx Config		_			·			
Rx Config L	ayer PPP IP	PayLoad Traffic Rate Im	pairments	Layer PPP IP Pay	Load			
Results	TP Selection			BERT Configuration		Sync Declare Settings	_	
Statistics	In percentin Ibota						-	
Port 2	Src TP Address	192 168 1 11	-	BER Pattern 2^9-1	Y	Sync Achieve Declare Count 64		
🖃 🤟 Bert - Rx	and a maaroos [172 - 100 - 1 - 11	_	21 User Defined Det	have 0 Langeth	Sync Loss Declare Count 1	1	
Tx Config	Dest IP Address	192 . 168 . 1 . 10		51 User Defined Pad			1 I I I	
Rx Conrig			-		3 💌 bits	Sync Loss Declare Window 1000		
Statistics	Auto Inc Dest IP	Range 10		All Ones All Zeros	0	Restore Default		
Statistics :	Doculto		a x	· · · · · · · · · · · · · · · · · · ·				
:	Kesuics			Statistics				Ť ^
P	ort Selection Port 1	Reset Clear LE	D History Insert Error	Port Selection Port 1	Reset Rx			
E	Bert Status			Tx	Values	Rx	Values	
R	Xx No Traffic	Not Active		Frame count	-	Total frame count	925822	
S	iync Loss	Not Active		Byte count	-	IPv4 frame count	925822	
B	Sit Error	Not Active				IP checksum error count	0	
<u> </u>	out of Sequence Packet	 Not Active 				IPv6 frame count	0	_
						Non IP test frame count	0	
E	Bert Statistics	Values				IP data over IP layer frame count	0	
в	ERT Status	SYNC		-		UDP data over IP layer frame count	925823	
Т	est Time	00:00:32				ICP data over IP layer frame count	0	
N	lo Rx Data Count	0				ICMP data over IP layer frame count	0	
N	lo Rx Data Seconds	0				IGDD data over ID laver frame count	0	
В	lits Received	259135200				Other data over IP laver frame count	0	
В	Bit Error Count	0				LIDP checksum error frame count	0	
B	lit Error Rate	0.0000E+000				UDP frame count	0	
В	lit Error Seconds	0				Non UDP test frame count	0	
Start Ty Stop Ty	Out Of Seq. Count	0						
Sources Sobus	ync Loss Count	0						
Start Rx Stop Rx	irror Eree Seconds	22						
	anor mee beconds	55						_

Figure: PoS BERT

PoS Tx / Rx Test

An emulation and test capability that transmits fixed, random, or variable lengths test packets and checks packets on receive at a user specified data transmission rate.

POS Tx/Rx Test					×
Tx Port Rx Port	Statistics				
	Packets	5 973	Packets [5 841
Length without FCS Fix/Var Packet Length					
Min: 20 Fixed Var. Increment	Bits/Sec	4 070 880	Bits/Sec		3 980 416
Max: 1000 Var. Random	Pkts/Sec	990	Pkts/Sec		968
Fixed: 203	Percent	2.739	Percent		2.678
Tx Config (max 148.608 Mbps)	Results Rx Seq Ei	ror Count 0			
Bits / Sec Percent 4 080 000 2.767	Tx Overn	un Count	0	un Count	0
Prepend Fixed Length Header Octets (Hex)		Buckets			
	Packet Length	Total Co	unt Error	Count	Err %
	1-10		0	0	0.000
	51-200		200	0	0.000
Rx Error Statistic Length Buckets (space separated)	201-500	18	300	0	0.000
10 50 200 500 2000 None	501-2000	29	955	0	0.000
Default ->	2001-8000		0	0	0.000
	,			· · ·	
Start Stop Insert Error	Reset Errors	Exit			

Figure: PoS Tx/Rx Test



ATM Analyzer– Asynchronous Transfer Mode Over SONET / SDH

Overview

ATM over SONT/SDH— OC-3/STM-1 and OC-12/STM-4 is supported at full rates. Access, capture, analysis, and emulation of ATM cells at wirespeed make this interface capability applicable for wide ranging next generation networks.

ATM Protocol Analyzer

ATM Analyzer is used to analyze and view ATM protocols across the U-plane for both NNI and UNI interface carrying AAL0, AAL2 and AAL5 traffic.

UMTS Protocol Analyzer

UMTS analyzer is capable of capturing, decoding and performing various test measurements across various interfaces i.e. lub, lur, luCs and luPs interfaces of the UMTS network. In addition, it supports ATM as the transport layer. It helps in fault diagnosis and troubleshooting UMTS network.

P AT	M Prote	ocol Analysi	s AAL2,5(UNI3.1)										III.				
Ele	⊻jew C	apture Stat	istics Database C	al Detail Be	ecords 🤉	onfigure	Help										
1	é 1	<i>4</i> 0	a 📲 🏭 📟		99 H	L HL 3	 % 🛒	Z\$ Z	D 61 PDa	0	Go	To					
Dev	TS	Frame#	TIME (R	elative)	Len		Error VPI	VCI	PT	OSF	AAL Type	Frame Ty	CID	U	UUI	CPI	5.
$\sqrt{2}$	30	9	00.00.00.033	399500	53		1	56	1		AAL5	CPS-Frame				0	
12	30	10	00:00:00.034	380625	53		1	72	1		AAL5	CPS-Frame				0	
12	30	11	00:00:00.050	399250	149		1	56	0		AAL5	CPS-Frame				0	
1 2	30	12	00:00:00.053	439458	101		1	40	0		AAL5	CPS-Frame				0	
1 2	30	13	00:00:00.055	400458	101		1	40	0		AAL5	CPS-Frame				0	
12	30	14	00:00:00.061	400500	53		1	40	1		AAL5	CPS-Frame				0	
1 2	30	15	00:00:00.062	040917	53		1	40	1		AAL5	CPS-Frame				0	-1
40		10	00.00.00.000	annon te	61			60			1410	coc r				0	- É
Provide the second seco	P yload dding CS Us anon ngth	er-to_Us Part Ind	5 Reasseably er Indication icator (CPI)	(CPCS-	PDU) I -UU)	ayer -	1 (56 (. 0 ×4F00 ×0102 00000 00000 12 (x	000001 0000001 000100 000 (0 000 (0 000 (0 000 (0	0 0000)) 0000000 2B0001))	0011 100 650B0000 03002440)))2&200000	00004010	5F9FI	FFE05	FFE29	0000	
Hex	Dump	of the F	rame Data														-
00 1	0 03	82 4F 00	00 00 01 00	00 00	65 OB	00 00	+	0	+	-							
01 0	2 00	01 00 2B	00 01 03 00	24 40	2A 20	00 00		+	\$ 9 *								
00 0	0 40	10 5F 9F	FF E0 5F FE	29 00	00 00	00 00	9	_ ÿà_	þ)								
OC 2	3 A0	7F E9						é									. Č
Off-lin	e Viewing	,			C:\Do	cuments ar	nd Settings	Sameer M	Nutal 28 Fr	ames			_				-

Figure: ATM Protocol Analyzer

ATM Configuration

ATM Configuration allows user to either pass or drop the Idle cells at the receiving stream.



Figure: ATM Port Configuration



ATM BERT

Support for the following PRBS Patterns: 2⁹ -1, 2¹¹ -1, 2¹⁵ -1, 2²⁰ -1, 2²³ -1, 2²⁹ -1, 2³¹ -1, All one's, all zero's, alternate ones and zeros, user defined pattern of lengths from 2 to 32 bits, invert and non-invert selections, single bit error insertion, error insert rate from 10⁻¹ to 10⁻⁹, HEC error insertion, on receive filtering is provided for idle cells, GFC, VPI, VCI, CL, and PT cells, statistical details for total cells, valid cells, idle cells, filtered cells, and filtered out cells.

- ATM Bert - [Untitled]										_ 🗆 🗵
- File View Windows I	Help									_ @ X
×	Ports: Port 1 •	-								
Configurations	Tx Config			4×	Rx Config					Ψ×
Port 1 Tx Config Results Port 2 Port 3 P	Port Selection Port 1 Layer ATM Header BERT Configuration BER Pattern 2015-1 31 User Define All Ones All Zero	PayLoad Traffic Rate II Ad Pattern 0 Len	settings mpairments gth y bas		Port Selection F Layer Recv Filt BERT Configura BER Pattern 2 31 User All Ones A	ort 2 PayLoad tion 15-1 Defined Pattern Zeros 0	x Rx coupled settin	Sync Declare Sett Sync Achieve Dec Sync Loss Decla Sync Loss Decla Restor	ings dare Count 64 lare Count 1 re Window 1000 re Default	
	I Invert Pattern				I Invert Patte					
1	Results			Ψ×	Statistics					4 ×
	Port Selection Port 1	Reset Clea	ar LED History Insert Error		Port Selection	ort 1 💌 Rese	t Rx			
	Bert Status				Tx	Values		Rx	Values	
Start Tx Stop Tx	R× No Traffic	Not Active			Frame count			Total cell count	2912921	
Start R.x Stop Rx	Sync Loss Bit Error	Not Active Not Active			Byte count	-		Idle cell count BER test cell count Filtered out cell count HEC error count	0 2912922 0 0	
	Bert Statistics	Values								
	BERT Status	SYNC			L					
	Test Time	00:01:21			L					
	No Rx Data Count	0			L					
	Bits Received	1105843832								
	Dit France Count	0								
	Bit Error Count	0								
	Bit Error Rate	0.0000E+000			L					
	Bit Error Rate Bit Error Seconds	0.0000E+000 0								
	Bit Error Rate Bit Error Seconds Sync Loss Count	0.0000E+000 0 0								

Figure: ATM BERT

ATM Tx / Rx Test

An emulation and test capability that transmits ATM test cells and / or analyzes the received cells at a user specified data transmission rate

ATM Tx/Rx Test	×
Tx Port User/Network Interface	Tx Config (max 148 Mbps, 353 Kcps) Start Cels/Sec 30000 Bits / Sec Percent 12 720 000 8,494 Timer /33 ms Exit
VPI 20 Virtual Path Identifier (0-255) VCI 655 Virtual Channel Identifier (0-65535) PT 0 Payload Typel: (0-7)	Statistics Rx Tx Test Cells 122 760 Bits/Sec 12 623 328 Bits/Sec 0 Bits/Sec 29 772 Cells/Sec 0 Depart 8.429 Depart 0
CLP Gel Loss Priority (0-1)	Results Rx Seq Resync Count 0 Rx Seq Error Count 0 Tx Overrun Count 0 Rx DTE Error Count 0 Rx DTE Error Count 0

Figure: ATM Tx/Rx Test

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Other Applications in LightSpeed1000[™] Analyzer

Record, Playback Packets and Cells

These modules allow users to transmit and capture packets from file or to a file over OC-3/STM-1 and OC-12/STM-4 interfaces. Offline utility can convert it into GL's HDL file format or PCAP format.

Transmit Packets from File

- Transmits packets / cells from the file
- Packets can be transmitted either continuously, limited by number of packets/cells, or till the end of file (EOF)
- Transmit packets/cells at a user configurable rate
- Transmits on the same port as captured, swaps ports or uses a specified port
- Provides the statistics of the transmitted cells at both line level and payload level
- Transmit packets synchronously on multiple boards

Receive Packets to File

- Hardware provided **versatile multiple filters** can be applied to incoming data on each individual port to allow traffic of interest only. ATM and PoS traffic can be filtered at hardware level to target traffic of interest only
- Allows Wirespeed capture of all payload from SONET/SDH envelop transparent of transport level
- Captures the received packets synchronously on multiple boards into a file up to hard drive capacity
- Packets can be captured continuously (till user manually stops the capture or up to hard drive capacity) or limited by a specified size in MB, a packet count, or a specified time limit

	2	D:\LIGHT_S	PEED TEST DATA\atrm\c	c3 1000 padet	
		Input File Cell	s Inp	ut File Capture Ports	
		1 000	k		
	All selected ports must reside on a single board	Transmission L	Init 10 C Packets C	EOF Continuous	
	Tx Config (max 148	Mbps, 350 Kcps) —	File to Tx Port Pack	et Routing	
	Estimated Packet	Length (POS)	€ Same C	Swap Ports (0<->1) s on Single Port	
	Cells (Packets) / S	Second	Statistics		
		35300	Tx Cells	143 220	
	Bits / Second	14 967 200	Cells/Sec	34 705	
	Percent		Bits/Sec	14 714 920	
		9,994	Percent	9.902	
			Synchronous Mult	i-Board Transmission art SMB Stop SMB	
[Start Stop	D Exit	Synchronous Mult	HBoard Transmission art SMB Stop SMB	
e Packets to F	Start Stop	p Exit	Synchronous Mult	Board Transmission	
e Packets to F	Start Stop	p Exit	Synchronous Mult	Board Transmission art:SMB Stop SMB	
e Packets to F	Start Stop	p Exit	Synchronous Mult	+Board Transmission art: SMB Stop SMB	.1
e Packets to F	Start Stop	p Exit	Synchronous Mult SMB Tx St SMB Tx St Alatrm\test1.DAT	+Board Transmission art: SMB Stop SMB	
e Packets to F	Start Stor File Output File File Name D:\LIGHT_S Output File	p Exit	Synchronous Mult	+Board Transmission art: SMB Stop SMB	
e Packets to F	Start Stor File File Name D:\LIGHT_S Output File Output File	p Exit SPEED TEST DAT Limit	A\atrm\test1.DAT	Hoard Transmission art SMB Stop SMB	Continuous
e Packets to F	Start Stor File Output File D:\LIGHT_S Output File Output File Output File	p Exit SPEED TEST DAT Limit C Indicators	Synchronous Mult	Heard Transmission art SMB Stop SMB	
e Packets to R	Start Stor File Output File D:\LIGHT_S Output File Output File Output File Output File Output File Output File Output File Output File	p Exit SPEED TEST DAT Limit Indicators tes/Sec Disk	Synchronous Mult SMB TX St Alatrmitest1.DAT Size MB C Par KWhite MT Buffer Ut	Heard Transmission	Continuous
e Packets to R	Start Stor File Output File D:\LIGHT_S Output File Output File Output File Output File Disk Write By 959 092	p Exit SPEED TEST DAT Limit Indicators tes/Sec Disk	Synchronous Mult SMB TX St Alatrm\test1.DAT Size MB C Par Write MT Buffer Ut	Heard Transmission art SMB Stop SMB Stop Stop Stop Stop Stop Stop Stop Stop] Continuous
e Packets to R ceive Ports	Start Stor File Output File File Name D:\LIGHT_S Output File 00:01:00 Performance I Disk Write By 959 092 File	p Exit	A\atrm\test1.DAT	-Board Transmission art SMB Stop SMB art SMB Stop SMB Stop SMB Stop SMB art SMB Stop SMB Stop SMB Stop SMB Stop SMB Stop SMB art SMB Stop SMB S	Continuous

Figure: Receive Packets to File, Transmit Packets from File

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Software Loopback (Rx-To-Tx Memory Loopback)

This application is used for diagnostic purposes. It loops all the received packets / cells from the SONET to the transmitting ports and displays the Tx and Rx information. Memory Loopback application uses both ports on the selected board.

and the second second	to oppose	CK	<u>, 11</u>		
Rx Unde	rRuns C	Sele Source (Rx)	ct Port(s) — Destinati 1,2	ion (Tx)	Start
	(ī l			Stop
Packe	et Mode	Skip Rx and Tx OnT	ïmer (pause >	cmit)	
' Page × inform	Mode nation	Flush Tx After Each	Packet Tx (p ⊤Tx inform	acket mode) nation	
[Packets	Bytes	Port	Packets	Bytes
Port	FOLNELS	07002			
1,2	1 836 430	102 840 080	1,2	1 836 430	102 840 080
x Bytes	1 836 430	102 840 080	1,2	1 836 430	102 840 080
1,2 1,2 tx Bytes	Avail LB:	102 840 080	1,2	1 836 430	102 840 080
x Bytes x Free S x Free -	1 836 430 Avail LB: ipace LB: Rx Avail:	102 840 080 102 840 080 16 52 260 879 52 260 863	1,2	1 836 430	102 840 080
tx Bytes x Free S x Free -	Avail LB: ipace LB: Rx Avail:	102 840 080 102 840 080 16 52 260 879 52 260 863 638 992	1,2	1 836 430	102 840 080

Figure: Memory Loopback

Alarms and Errors Counters Monitoring

The alarms and error monitoring window provided for each of the OC-3/OC-12 port displays detailed status of the communication with the other end.

Hardware LEDs are provided on the card to read line alarms.

Monitored Alarms and error counts include -

- Line errors such as OOF, LOS, LOF, AIS, RDI, and APSBF
- FCS, Rx / Tx Abort, and MIN / MAX Length
- Line, Path, and Section error counts





SONET/SDH RAW (or Transparent) Payload

RAW mode captures or playbacks anything and everything on SONET/SDH. This mode allows capturing/replaying including SONET/SDH Framing and payload. Here payload can be anything, including structured traffic (T1, E1, STS-1, DS3 etc) or unstructured traffic (ATM, PoS, GFP etc). Raw or transparent mode allows direct access to the SONET / SDH payload for BERT, data transmit and receive applications. Current applications include:

- RAW BERT support for the following PRBS Patterns: 2⁹ 1, 2¹¹ 1, 2¹⁵ 1, 2²⁰ 1, 2²³ 1, 2²⁹ 1, 2³¹ 1, all one's, all zero's, alternate ones and zeros, user defined pattern of lengths from 2 to 32 bits, invert and non-invert selections, single bit error insertion, error insert rate from 10⁻¹ to 10⁻⁹, status for pattern sync, and bit errors counters
- Wirespeed capture of raw data to hard disk on one or both ports simultaneously. The data is recorded in 64 bytes block with appropriate header
- Playback of recorded data from file at wirespeed on one or both ports
- Alarms and Error monitoring and logging at SONET/SDH level

Performance Counters

Following performance counters are available in the analyzer: Tx Statistics, Rx Statistics, PMC TxRx Statistics, Interrupt Statistics, and DMA Engine. The statistics display two types of counters: board counters and port counters. The board counters display cumulative counts for all ports on the same board, while port counters display information for each port separately.

× Descripl × Descrip	Interrupt S Descript Reation Aps Aps Aps Aps Aps Aps Aps Aps Aps Aps	atistics	lics			×	X	
Laps	DMA RX Inb DMA Timer 1	Board C	Rx Statistics				×	
Buffer L	DMA TX Inte	DMA Eng	Board Counters		Board 1			
Buffer 1	DMA RX Inb DMA Timer 1	PC Memc	DMA Engine PCI	e Packets	192 688 918			
x Buffer I x Buffer I x Buffer I	Statis DTE GigE	DMA Engine PCI	e Pgs	3 391 681				
	INTF Gig	DTE Packets		192 195 103				
	INTE Go	INTE GIGE PKTs		3 735 936 685				
	ann ag	INTE GigE Errore	ed PKTs	3 735 936 685				
		INTF GigE Pkts p INTF GigE Max L		en PKTs	3 735 936 685			
			INTF GigE Min Le	en PKTs	3 735 936 685			
	Port Cou							
		Port Cou		PMC Tx/Rx	Statistics			
		Port Cou DTE Paci INTF Pac	Port Counters	PMC Tx/Rx	Statistics			
		Port Cou DTE Paci INTF Pac INTF Erro	Port Counters	PMC Tx/Rx	Statistics	Port 1	Port 2	
		Port Cou DTE Paci INTF Pac INTF Errc INTF Pac	Port Counters DTE OC-3/12 I INTF OC-3/12	PMC Tx/Rx Port Counter TX cels	Statistics s	Port 1 4 996 949	Port 2	
		Port Cou DTE Pac INTF Pac INTF Errc INTF Pac	Port Counters DTE OC-3/121 INTF OC-3/12 INTF OC-3/12 INTF OC-3/12	PMC Tx/Rx Port Counter TX cells RX idle cells	Statistics	Port 1 4 996 949	Port 2 187 203 069	
		Port Cou DTE Paci INTF Pac INTF Errc INTF Pac	Port Counters DTE OC-3/12 I INTF OC-3/12 INTF OC-3/12 INTF OC-3/12 INTF OC-3/12	PMC Tx/Rx Port Counter TX cells RX idle cells RX cells	Statistics	Port 1 4 996 949 960 059 015 187 240 772	Port 2 187 203 069 1 138 319 674 5 427 366	
		Port Cou DTE Pacl INTF Pac INTF Errc INTF Pac	Port Counters DTE OC-3/121 INTF OC-3/12 INTF OC-3/12 INTF OC-3/12 INTF OC-3/12 INTF OC-3/12	PMC Tx/Rx Port Counter TX cells RX idle cells RX cells RX HCS error	s s	Port 1 4 996 949 960 059 015 187 240 772 0	Port 2 187 203 069 1 138 319 674 5 427 366 4	
		Port Cou DTE Pad INTF Pac INTF Erro INTF Pac	Port Counters DTE OC-3/121 INTF OC-3/12 INTF OC-3/12 INTF OC-3/12 INTF OC-3/12 INTF OC-3/12 Filtered OC-3/ Filtered OC-3/	PMC Tx/Rx Port Counter TX cells RX idle cells RX cells RX HCS error	s s	Port 1 4 996 949 960 059 015 187 240 772 0	Port 2 187 203 069 1 138 319 674 5 427 366 4	
		Port Cou DTE Pad INTF Pac INTF Proc	Port Counters DTE OC-3/12 INTF OC-3/12 INTF OC-3/12 INTF OC-3/12 INTF OC-3/12 INTF OC-3/12 Fittered OC-3/ Fittered OC-3/ Fittered OC-3/ Fittered OC-3/	Port Counter TX cells RX idle cells RX cells RX HCS error	s s	Port 1 4 996 949 960 059 015 187 240 772 0	Port 2 187 203 069 1 138 319 674 5 427 366 4	
Refrect		Port Cou DTE Pad INTF Pac INTF Proc	Port Counters DTE OC-3/12 INTF OC-3/12 INTF OC-3/12 INTF OC-3/12 INTF OC-3/12 INTF OC-3/12 Fittered OC-3/ Fittered OC-3/ Fitter OC-3/12 Fittere OC-3/12 Fitter OC-3/12 Fitter OC-3/12	Port Counter TX cells RX idle cells RX HCS error	s s	Port 1 4 996 949 960 059 015 187 240 772 0	Port 2 187 203 069 1 138 319 674 5 427 366 4	
Refrest		Port Cou DTE Pad INTF Pac INTF Pac	Port Counters DTE OC-3/121 INTF OC-3/12 INTF OC-3/12 INTF OC-3/12 INTF OC-3/12 INTF OC-3/12 INTF OC-3/12 Filtered OC-3/ Filter OC-3/12 Filter OC-3/12 Filter OC-3/12 Ethere OC-3/12	PMC Tx/Rx Port Counter TX cells RX idle cells RX cells RX HCS error	s s	Port 1 4 996 949 960 059 015 187 240 772 0	Port 2 187 203 069 1 138 319 674 5 427 366 4	
Refrest	Refresh	Port Cou DTE Pad INTF Pac INTF Pac	Port Counters DTE OC-3/121 INTF OC-3/12 INTF OC-3/12 INTF OC-3/12 INTF OC-3/12 INTF OC-3/12 INTF OC-3/12 Filtered OC-3/ Filter OC-3/12 Filter OC-3/12 Filter OC-3/12 Ethere OC-3/12	PMC Tx/Rx Port Counter TX cells RX idle cells RX cells RX HCS error	s s	Port 1 4 996 949 960 059 015 187 240 772 0	Port 2 187 203 069 1 138 319 674 5 427 366 4	

Figure: Packet Delay Emulation

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Software Loopback (Rx-To-Tx Memory Loopback)

This application is used for diagnostic purposes. It loops all the received packets / cells from the SONET to the transmitting ports and displays the Tx and Rx information. Memory Loopback application uses both ports on the selected board.

		Sele	ct Port(s) —		
× Unde	rRuns	Source (R.x)	Destinati	ion (Tx)	
	(1,2	1,2		Start
x Over	Runs				
	(Stop
Packe	et Mode	Skip Rx and Tx OnT	imer (pause >	mit)	
Page	Mode	Flush Tx After Each	Packet Tx (p	acket mode)	
< inform	nation		Tx inform	nation	
Port	Packets	Bytes	Port	Packets	Bytes
1,2	1 836 430	102 840 080	1,2	1 836 430	102 840 080
		B			
Bytes	Avail LB:	16			
(Bytes	Avail LB: ipace LB:	16 52 260 879			
(Bytes	Avail LB: ipace LB: Rx Avail:	16 52 260 879 52 260 863			
< Bytes < Free S < Free -	Avail LB: Space LB: Rx Avail:	16 52 260 879 52 260 863			
< Bytes < Free S < Free -	Avail LB: ipace LB: Rx Avail:	16 52 260 879 52 260 863			
< Bytes < Free S < Free - < Bytes	Avail LB: ipace LB: Rx Avail: Available:	16 52 260 879 52 260 863 638 992 53 800 855			

Figure: Memory Loopback

Packet Delay Emulation for PoS and ATM based traffic

The Network Delay Emulator is an optional application (requires license) provides full duplex delay simulation for PoS and ATM based traffic from 1 ms to 500 ms, with incremental delays of 1 ms. The application combines hardware and software based functions to achieve precision and flexibility. It can emulate packet delays that occur over SONET/SDH carrying ATM/PoS traffic.

With this application, the user can:

- Test the impact of delay and congestion under various real world conditions
- Assess impact of delay on SLA (Service Level Agreements),
- Simulate satellite delay and long Fiber Loops
- Test WAN application performance under deteriorated but repeatable conditions



Figure: Packet Delay Emulation

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Supported Protocols

- ATM Implements the ATM Forum User Network Interface Specification and the ATM physical layer for Broadband ISDN according to CCITT Recommendation 1.432
- **PPP over SONET (PoS)** Implements the Point-to-Point Protocol (PPP) over SONET / SDH specification according to RFC 2615 (1619) / 1662 of the PPP Working Group of the Internet Engineering Task Force (IETF)
- OC-3/OC-12/STM-1/STM-4 Transparent Payload Analyzer processes SONET/SDH payload in transparent (RAW) mode without any transport protocols

Specifications

Interfaces:

- 2 x Unchannelized OC-3 / STM-1 / OC-12 / STM-4 Ports (Port 1 Port 2)
- 2 x Channelized OC-3 / STM-1 / OC-12 / STM-4 Ports (Port 3 Port 4)
- Single Mode or Multi Mode SFP support with LC connector

Protocols:

• POS compliance specs - RFC 2615(1619)/1662

Tx Clock

• Internal or Recovered

Alarm LEDs:

• LOS, LOF, User

Bus Interface:

- PCIe Specification
 - 1.2 Compliant
- USB 2.0

Power and Dimensions:

- +12 volts, 3.5 Amps
- 4.2" x 9.2"



Buyer's Guide

Item No	Product Description
<u>LTS100</u>	Lightspeed1000™ - Dual OC-3/12 STM-1/4 PCIe Card
LTS105	Lightspeed1000™ - Portable Dual OC-3/12 STM-1/4 USB Unit
IPN1310a	SFP Transceiver for OC-3/STM-1 and OC-12/STM-4 Optical, LC, Single-Mode, 1310nm
<u>IPN850a</u>	SFP Transceiver for OC-3/STM-1 and OC-12/STM-4 Optical, LC, Multi-Mode, 850 nm or 1310 nm

Item No	Unchannelized Analysis and Emulation Applications Related Software
<u>LTS200</u>	OC-3/STM-1 ATM Monitor, BERT, Tx/Rx Test, RAW
<u>LTS300</u>	OC-12/STM-4 ATM Monitor, BERT, Tx/Rx Test, RAW
<u>LTS201</u>	OC-3/STM-1 PoS Monitor, BERT, Tx/Rx Test, RAW
<u>LTS301</u>	OC-12/STM-4 PoS Monitor, BERT, Tx/Rx Test, RAW
<u>LTS202</u>	OC-3/STM-1 ATM and RAW Record / Playback
<u>LTS203</u>	OC-3/STM-1 PoS and RAW Record / Playback
<u>LTS302</u>	OC-12/STM-4 ATM and RAW Record / Playback
<u>LTS303</u>	OC-12/STM-4 PoS and RAW Record / Playback
<u>LTS204</u>	OC-3/STM-1 ATM Protocol Analysis
<u>LTS304</u>	OC-12/STM-4 ATM Protocol Analysis
<u>LTS206</u>	OC-3/STM-1 UMTS Protocol Analysis
<u>LTS306</u>	OC-12/STM-4 UMTS Protocol Analysis
<u>LTS215</u>	Packet Data Analysis (PDA) for PoS
<u>LTS207</u>	Delay Emulation for OC-3/STM-1 PoS payloads
<u>LTS208</u>	Delay Emulation for OC-3/STM-1 ATM payloads
<u>LTS307</u>	Delay Emulation for OC-12/STM-4 PoS payloads
<u>LTS308</u>	Delay Emulation for OC-12/STM-4 ATM payloads

GL Communications Inc.

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Buyer's Guide (Contd.)

Item No	OC-12 / STM-4 Related Software Related Hardware
<u>LTS501</u>	OC-3/STM-1 RAW
<u>LTS502</u>	OC-12/STM-4 RAW
<u>LTS503</u>	Record Playback for OC-3/STM-1 RAW
<u>LTS504</u>	Record Playback for OC-4/STM-4 RAW
<u>LTS108</u>	Any 16 Ports Channelized License for OC-3/STM-1
<u>LTS116</u>	Any 32 Ports Channelized License for OC-3/STM-1
<u>LTS124</u>	Any 48 Ports Channelized License for OC-3/STM-1
LTS132	Any 64 Ports Channelized License for OC-3/STM-1
LTS164	All Ports Channelized Licenses for OC-3/STM-1 (84x2 for T1, 63x2 for E1)

<u>Note</u>: PCs which include GL hardware/software require Intel or AMD processors for compliance.

For more details, refer <u>LightSpeed1000™</u> webpage.



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