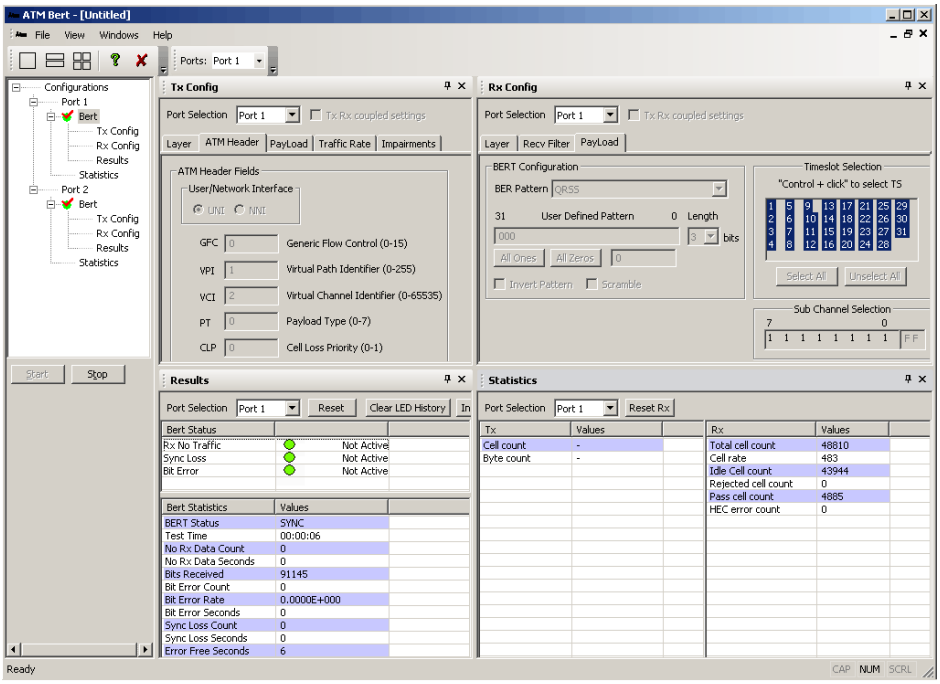
T1 E1 ATM BERT



Overview

GL's **T1 E1 ATM Bit Error Rate Test** (BERT) application permits BER testing across an ATM channel operating over PDH circuits. The application transmits a BERT pattern using the simplest ATM Adaptation Layer, i.e. AAL0. The BERT pattern is inserted in its entirety into the 48 byte payload of the cell. Cells are either "BERT payload" or "idle" cells. Note that "cell headers" and payload can overlap the framing position.

GL has various tools for the analysis and to test ATM. For example, ATM Analyzer, Inverse Multiplexing over ATM (IMA) Analyzer, T3 E3 ATM Analyzer, OC-3 STM-1 OC-12 STM-4 ATM Analyzer and many others.

Note: Currently this application is not available on Octal/Quad T1 /E1 Analyzers.

For more information, please visit T1 E1 ATM BERT webpage.

Main Features

- Capable of generating/receiving ATM traffic
- Support user-defined ATM header configuration for GFC, VPI, VCI, PT, CLP
- User-defined traffic rate to the accuracy of 1% of total bandwidth.
- Supports different QRSS, PRBS patterns 2^9-1, 2^{11}-1, 2^{15}-1, 2^{20}-1, 2^{23}-1,fixed patterns like All one's, All zero's, alternate 1's and 0's, 1:1, 1:7, and User -defined patterns. User defined patterns length can be 3 to 32 bits in length.
- Supports inverting, and scrambling payload data. Scrambling is according to ITU-T G.804
- Supports single bit error insertion, and error rate insertion.
- Provides ATM QoS measurement (Bit error count/ Rate/Seconds, Sync Loss, No Rx data,…)
- Provides ATM Statistics (total cell count, rejected / pass / idle cell counts, cell rate, and HEC error count).
- Error, and Alarm LEDs for easy analysis.
- Supports testing on multiple cards simultaneously with consolidated result view.
- Tx and Rx settings for multiple cards can be independently controlled or coupled.
- Capability to save and load the configuration settings.

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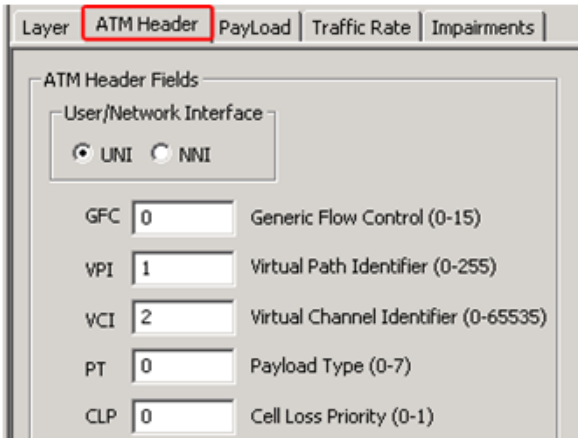
ATM Header Configuration

ATM layer provides configuration of ATM header fields such as GFC (Generic Flow Control), VPI (Virtual Path Identifier), VCI (Virtual Channel Identifier), PT (Payload Type) , and CLP (Cell Loss Priority). ATM header GFC (Generic Flow Control) field is enabled only for UNI interface. On the Rx side, user selectable Filters are provided, which are used to accept/reject incoming ATM cells.

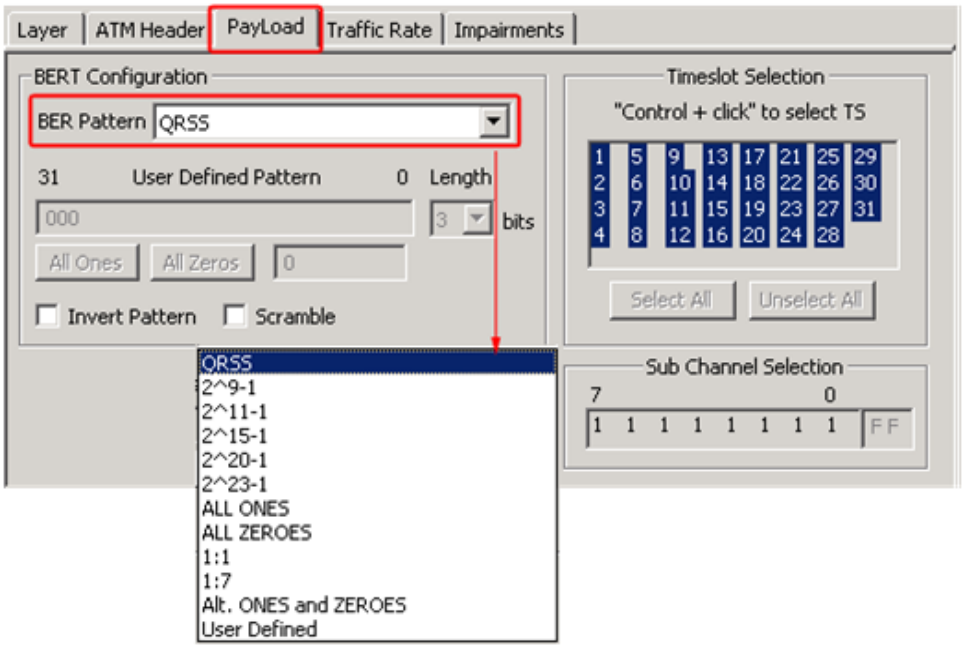


ATM Header Fields

BER Pattern Configuration

Payload at the Tx configuration allows user to select specific Bit Error Rate test pattern for transmission. T1/E1 ATM BERT support various BERT patterns; QRSS, PRBS patterns such as 2^9-1, 2^{11}-1, 2^{15}-1, 2^{20}-1, 2^{23}-1, fixed patterns such as all ones, all zeros, alternate 1s and 0s, and user-defined patterns. Other options such as invert and scrambling options (according to ITU-T G.804) are provided.

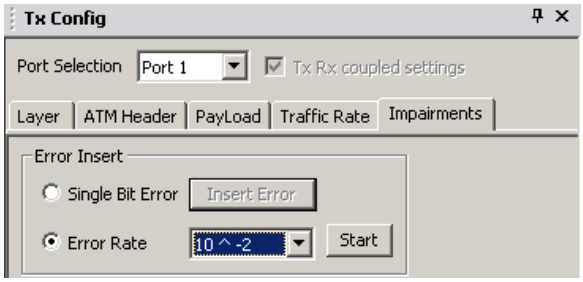
At Rx configuration these patterns are used to verify the incoming BERT pattern. Pattern Sync is achieved only if BERT pattern matches configuration options, configurable header length and header information.



Payload Generation

Bit Error Insertion

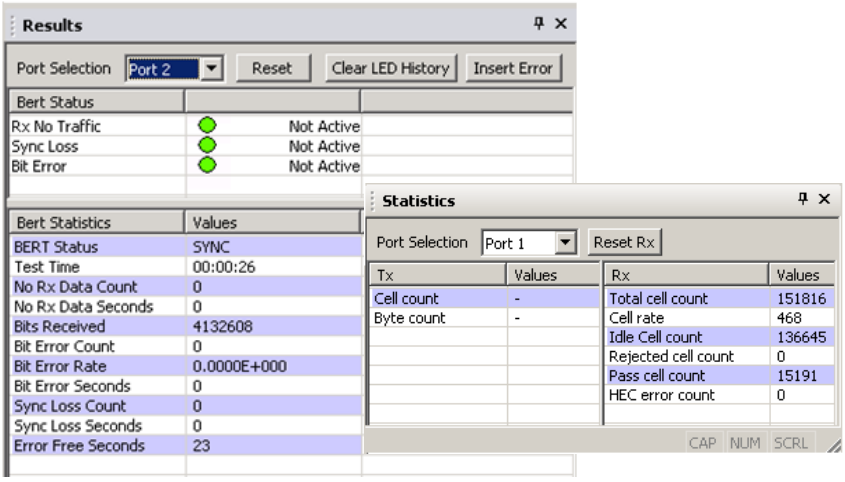
ATM BERT allows users to insert single bit error or error rate from 10^{-2} to 10^{-9} into the outgoing (TX) BERT stream.



Impairments

BERT Results and Tx/Rx Statistics

The Result screen displays both **BERT Status** and **BERT Statistics** such as count of no rx data, no rx data seconds, bits received, bit errors, bit error rate/seconds, sync loss count/seconds, and error free seconds. BERT Status provides a quick view of the BERT Test status in the form of Alarm LEDs.

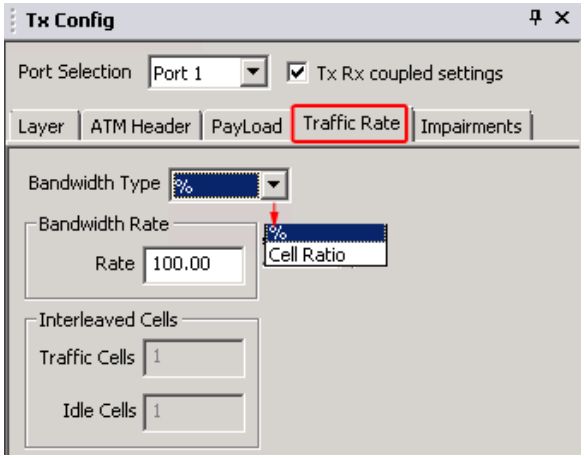


BERT Results and Statistics

Traffic Rate

The Traffic Rate to be generated can be configured in 2 ways:

- Percent of total bandwidth with range starting from 1 to 100%
- Cell Ratio, where users can set the ratio of ATM traffic cells to idle cells



Traffic Rate

Buyer's Guide

Item No	Product Description
XX162	T1 E1 ATM BERT

Item No	Related Software
XX160	T1 or E1 ATM Analyzer
XX022	DTMF/MF/MFR2 Detector and Generator Software

Item No	Related Hardware
PTE001	tProbe™ Dual T1 E1 Laptop Analyzer (Require Basic Software)
FTE001	QuadXpress T1 E1 Main Board (Quad Port)
ETE001	OctalXpress T1 E1 Daughter boards (Octal Port)
XTE001	Dual Express (PCIe) T1 E1 Boards
TTE001	tScan16™ T1 E1 Boards

Note: PCs which include GL hardware/software require Intel or AMD processors for compliance.

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