# T1 E1 ATM BERT

- ATM Bert - [Untitled]						- O ×			
File View Windows H	telp								- 8 ×
	Ports: Port 1 ▼								
Configurations	Tx Config		Ψ×	Rx Config					Ψ×
Port 1	Port Selection Port 1	Tx Rx coupled :		Port Selection Port Layer Recv Filte BERT Configuration	r PayLoad	Rx coupled	Ti	neslot Selection	тя
Port 2     Port Config     Port Config     Revits     Statistics	GET/HELWORK I REF GUNI C NNI GFC 0 VPI 1 VCI 2 PT 0 CLP 0	Generic Flow Control (0- Virtual Path Identifier (0 Virtual Channel Identifier Payload Type (0-7) Cell Loss Priority (0-1)	-255)		Zeros	0 Leng	th bits bits 7 540 7	13         17         21         22         26           13         14         18         22         26           15         19         23         27           2         16         20         24         28           All         Unselect         Unselect         0           Channel Selection         0         1         1         1	
Start Stop	Results		4 ×	Statistics					ąχ
	Port Selection Port 1	▼ Reset Clear	LED History In	Port Selection Po	rt 1 💌 Reset	Rx			
	Bert Status			Tx	Values		Rx	Values	
	R× No Traffic	Not Active		Cell count	-		Total cell count	48810	
	Sync Loss	Not Active		Byte count	-		Cell rate	483	
	Bit Error	Not Active					Idle Cell count	43944	
							Rejected cell count	0	
	Bert Statistics	Values					Pass cell count	4885	
							HEC error count	0	
	BERT Status Test Time	SYNC 00:00:06							
	No Rx Data Count	0:00:06							
	No Rx Data Seconds	0							
	Bits Received	91145							
	Bit Error Count	0							
	Bit Error Rate	0.0000E+000							
	Bit Error Seconds	0							
	Sync Loss Count	0							
	Sync Loss Seconds	0							
<b>▲</b>	Error Free Seconds	6							
Ready								CAP NUM	SCRL /

#### **Overview**

GL's **T1 E1 ATM Bit Error Rate Test** (BERT) application permits BER testing across an ATM channel operating over PDH circuits. The application transmits a BERT pattern using the simplest ATM Adaptation Layer, i.e. AALO. The BERT pattern is inserted in its entirety into the 48 byte payload of the cell. Cells are either "BERT payload" or "idle" cells. Note that "cell headers" and payload can overlap the framing position.

GL has various tools for the analysis and to test ATM. For example, <u>ATM Analyzer</u>, <u>Inverse Multiplexing over ATM (IMA) Analyzer</u>, <u>T3 E3</u> <u>ATM Analyzer</u>, <u>OC-3 STM-1 OC-12 STM-4 ATM Analyzer</u> and many others.

Note: Currently this application is not available on Octal/Quad T1 /E1 Analyzers.

For more information, please visit <u>T1 E1 ATM BERT</u> webpage.

## **Main Features**

- Capable of generating/receiving ATM traffic
- Support user-defined ATM header configuration for GFC, VPI, VCI, PT, CLP
- User-defined traffic rate to the accuracy of 1% of total bandwidth.
- Supports different QRSS, PRBS patterns 2<sup>9</sup>-1, 2<sup>11</sup>-1, 2<sup>15</sup>-1, 2<sup>20</sup>-1, 2<sup>23</sup>-1, fixed patterns like All one's, All zero's, alternate 1's and 0's, 1:1, 1:7, and User -defined patterns. User defined patterns length can be 3 to 32 bits in length.
- Supports inverting, and scrambling payload data. Scrambling is according to ITU-T G.804
- Supports single bit error insertion, and error rate insertion.
- Provides ATM QoS measurement (Bit error count/ Rate/Seconds, Sync Loss, No Rx data,...)
- Provides ATM Statistics (total cell count, rejected / pass / idle cell counts, cell rate, and HEC error count).
- Error, and Alarm LEDs for easy analysis.
- Supports testing on multiple cards simultaneously with consolidated result view.
- Tx and Rx settings for multiple cards can be independently controlled or coupled.
- Capability to save and load the configuration settings.

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### **ATM Header Configuration**

ATM layer provides configuration of ATM header fields such as GFC (Generic Flow Control), VPI (Virtual Path Identifier), VCI (Virtual Channel Identifier), PT (Payload Type), and CLP (Cell Loss Priority). ATM header GFC (Generic Flow Control) field is enabled only for UNI interface. On the Rx side, user selectable Filters are provided, which are used to accept/reject incoming ATM cells.

Layer	ATM Header	PayLoad	Traffic Rate	Impairments
_Us	Header Fields – er/Network Inte UNI C NNI	erface -		
	GFC 0	Gener	ic Flow Control	(0-15)
	VPI 1	Virtua	l Path Identifie	r (0-255)
	VCI 2	Virtua	l Channel Ideni	tifier (0-65535)
	PT 0	Payloa	ad Type (0-7)	
	CLP 0	Cell Lo	oss Priority (0-1	)

**ATM Header Fields** 

## **BER Pattern Configuration**

Payload at the Tx configuration allows user to select specific Bit Error Rate test pattern for transmission. T1/E1 ATM BERT support various BERT patterns; QRSS, PRBS patterns such as 2<sup>9</sup>-1, 2<sup>11</sup>-1, 2<sup>15</sup>-1, 2<sup>20</sup>-1, 2<sup>23</sup>-1, fixed patterns such as all ones, all zeros, alternate 1s and 0s, and user-defined patterns. Other options such as invert and scrambling options (according to ITU-T G.804) are provided.

At Rx configuration these patterns are used to verify the incoming BERT pattern. Pattern Sync is achieved only if BERT pattern matches configuration options, configurable header length and header information.

Layer ATM Header PayLoad Traffic Rate Impairments	;
BERT Configuration	Timeslot Selection
BER Pattern QRSS	"Control + click" to select TS
31     User Defined Pattern     0     Length       000     3     v     bits       All Ones     All Zeros     0       Invert Pattern     Scramble	1       5       9       13       17       21       25       29         2       6       10       14       18       22       26       30         3       7       11       15       19       23       27       31         4       8       12       16       20       24       28         Select All
OR55 2^9-1	Sub Channel Selection
2^11-1	7 0 1 1 1 1 1 1 1 1 FF
2^15-1 2^20-1	[] [] ·
2^23-1 ALL ONES ALL ZEROES 1:1 1:7 Alt. ONES and ZEROES User Defined	

**Payload Generation** 



### **Bit Error Insertion**

ATM BERT allows users to insert single bit error or error rate from 10<sup>-2</sup> to 10<sup>-9</sup> into the outgoing (TX) BERT stream.

Tx Config	<b>џ</b>	×
Port Selection Port 1 🔽 🕅 Tx Rx coupled settings		
Layer ATM Header PayLoad Traffic Rate Impairments		
Error Insert		
C Single Bit Error Insert Error		
Error Rate		
· · ·		

Impairments

## **BERT Results and Tx/Rx Statistics**

The Result screen displays both **BERT Status** and **BERT Statistics** such as count of no rx data, no rx data seconds, bits received, bit errors, bit error rate/seconds, sync loss count/seconds, and error free seconds. BERT Status provides a quick view of the BERT Test status in the form of Alarm LEDs.

Port Selection Port 2	Reset Clea	r LED History	nsert Error		
Bert Status					
R× No Traffic	Not Active				
Sync Loss	Not Active				
Bit Error	<ul> <li>Not Active</li> </ul>				
		Statistics			<b>д</b> >
Bert Statistics	Values				
BERT Status	SYNC	Port Selection	Port 1 💌	Reset Rx	
Test Time	00:00:26	Tx	Values	Rx	Values
No Rx Data Count	0				
No Rx Data Seconds	0	Cell count	-	Total cell count	151816
Bits Received	4132608	Byte count	-	Cell rate	468
Bit Error Count	0			Idle Cell count	136649
Bit Error Rate	0.0000E+000	l		Rejected cell count Pass cell count	0
Bit Error Seconds	0	1			15191
Sync Loss Count	0	I		HEC error count	0
Sync Loss Seconds	0	1		1	
Error Free Seconds	23			CAP NUM	SCRL

**BERT Results and Statistics** 

## **Traffic Rate**

The Traffic Rate to be generated can be configured in 2 ways:

- Percent of total bandwidth with range starting from 1 to 100%
- Cell Ratio, where users can set the ratio of ATM traffic cells to idle cells

Tx Config	<b>₽</b>	×
Port Selection Port 1 💌 🗹 Tx Rx coupled settings		
Layer ATM Header PayLoad Traffic Rate Impairments	1	
Bandwidth Type <b>7</b> Bandwidth Rate Rate 100.00		
Interleaved Cells		
Traffic Cells 1		
Idle Cells 1		

**Traffic Rate** 



#### **Buyer's Guide**

ltem No	Product Description
<u>XX162</u>	T1 E1 ATM BERT
Item No	Related Software
<u>XX160</u>	T1 or E1 ATM Analyzer
<u>XX022</u>	DTMF/MF/MFR2 Detector and Generator Software
Item No	Related Hardware
<u>PTE001</u>	tProbe™ Dual T1 E1 Laptop Analyzer (Require Basic Software)
ETE001	QuadXpress T1 E1 Main Board (Quad Port)

<u>FTE001</u>	QuadXpress T1 E1 Main Board (Quad Port)
<u>ETE001</u>	OctalXpress T1 E1 Daughter boards (Octal Port)
<u>XTE001</u>	Dual Express (PCIe) T1 E1 Boards
<u>TTE001</u>	tScan16™ T1 E1 Boards

Note: PCs which include GL hardware/software require Intel or AMD processors for compliance.

For more information, please visit <u>T1 E1 ATM BERT</u> webpage.



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