

Supports M23 and C-bit Framing Format

DS3/DS1/DS0 Test and Analysis with UltraT1/E1

T3 line frequency and level measurement

Non-Intrusive Monitor for Alarms and Errors

Drop and Insert User Selected T1/E1

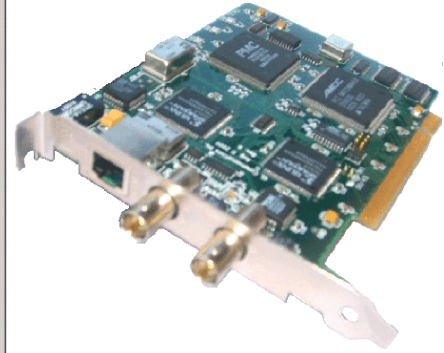
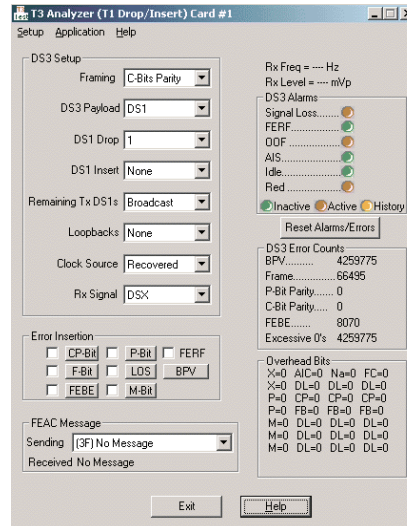
Broadcast or Looped back individual DS1/E1

Decode and Simulate FEAC And FDL Messages

Compatible with GL's T1/E1 Test Products

Real-time display of DS3 signaling bits

T3 Analyzer



A DS3 line (also known as a T3) is an ultra high-speed connection capable of transmitting data at rates up to 45 Mbps. A DS3 signal carries 28 T1 signals, each operating at a rate of 1.544 Mbps.

The GL's UltraT3 Cards (PCI) plug into PC expansion slot and provide digital T3 input/output for analyzing, testing, simulating, and monitoring T3 signals. A single T1/E1 input and output is provided to insert and receive T1 (or E1) signals into the T3 stream. The cards provide the capability of generating 28 DS1 or (21 E1) signals within the DS3 output.

The T3 Card when used in conjunction with Ultra T1 Card in same PC provides a complete DS3, DS1, and DS0 testing solutions.

The DS3 Receiver non-intrusively monitors a DS3 bit stream, and presents comprehensive diagnostics of PCM impairments and alarm messages in real-time. The input is compatible with the signal found at the DSX-3 panel, as well as at the output of a DS3 source. The user selected DS1 (or E1) is dropped or inserted at the T1/E1 output interface provided on the T3 Card.

The DS3 Transmitter can multiplex an externally supplied DS1 (or E1) bit stream into the DS3 signal. Designed to stress test M13 multiplexers and 3/1 Digital Cross Connect System.

Main Features

- User-friendly graphical software for comprehensive monitoring and testing of a T3 line.
- M23 and C-bit Framing Format
- Adding/Dropping a selected DS1 signal to/from the DS3 signal.
- Monitoring all DS3 alarms.
- Error insertion and error counting for all major DS3 error types.
- Transmit/Receive User selected T1 (or E1) while remaining T1s (or E1s) are Looped Back or Broadcast
- Real-time display of DS3 signaling bits.
- Non-Intrusive Monitoring and Time-Stamped Logging of all alarms and abnormal events
- Unframed T3 Bit Error Rate Testing with Detailed Logging.
- T3 line frequency and level measurement.
- Interface options for T3 termination or T3 monitoring.
- Clock option for internal or recovered clock.
- Transmission and reception of Far End Alarm Channel (FEAC) codes (optional software)
- Transmission and reception of Terminal Path Maintenance Data Link (MDL) (optional software)

For more details, visit <http://www.gl.com/ultrat3.html>



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Product specifications for the Ultra T3 Card

Mechanical Specifications

PC Interface PCI 2.1
Card Dimensions 5.5 in. x 4.2 in
DS3 Interface BNC Connectors
DS1 Interface RJ48c Connector

DS3 Line Interface

Output Amplitude: 800mV ± 50mV
Output Clock Source: Internal oscillator, or recovered from input DS3
Internal Clock Freq.: 44.736MHz ± 5ppm
Receiver Interface: DSX-3 (Termination or Monitor)
Input Impedance: 75 Ohm
Line Code Format: B3ZS
Terminate Input Level: 0.09Vp – 0.85Vp
Monitor Input Level: 0.025Vp – 0.08Vp

DS1 Line Interface

Output Amplitude: 3.0V ± 0.2V
Output Clock Source: Recovered from a demultiplexed DS1
Line Code Format: B8ZS (present and future releases); AMI (future releases)
Receiver Interface: DS1 Termination
Input Impedance: 100 Ohm
Input Level: 75mVp to 6.0Vp (–30dBsX to +6dBsX)

DS3 Framing Format

DS3 uses two framing formats: **M23** and **C-bit Parity**. The standards are defined as per ANSI T1.107-1995.

M23 multiplexer accepts seven DS2 inputs from seven separate DS2 multiplexers to produce a DS3 signal in the M23 format.

C bit Parity is a T3 framing structure that uses the control bits (C bits) for additional functions such as Far End Alarm Channel (FEAC), Far End Block Errors (FEBE), Terminal Data Link (TDL), C-bit Parity (CP). The FEAC-bit holds the Far-End Alarm and Control (FEAC) channel used for transmitting far-end status and alarm conditions to the near-end terminal. The T3 analyzer allows FEAC channel to be used for sending loop back requests and replies.

DL-bits the terminal-to-terminal path Maintenance Data Link (MDL). This link is also sometimes called the Facility Data Link (FDL). DS3 equipment uses the LAPD protocol to send messages on this link and so the messages are encoded in HDLC frames. The T3 analyzer allows transmission and reception of these MDL messages as shown in the figure across.

DS3 Transmitter

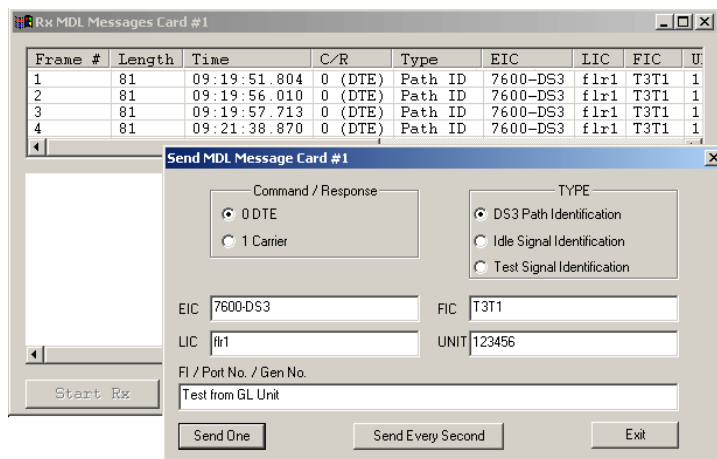
Payloads: Framed DS3, Unframed BERT pattern, AIS, Idle
Framing formats: M23, C-bit Parity
DS1 payloads: DS1 received at RJ48c jack, DS1s dropped from input DS3, AIS
BERT patterns: 2²³-1 (present and future releases); 2²⁰-1, 2¹⁵-1, 1100, 1010, 1000, all 1's, all 0's, user defined 24-bit pattern (future releases)
Error Insertion: FERF, FEBE, P-bit, CP-bit, M-bit, F-bit, Line Code Violation, Loss of Signal.
Loop backs: Complete DS3 signal, Selected DS1s from inbound DS3

DS3 Receiver

Framing formats: M23, C-bit Parity, Unframed (only for BERT)
DS1 Drop: Drop selected DS1 to RJ48c jack
Signal monitors: Input frequency (5ppm accuracy), Input level
Alarm monitors: Loss Of Signal, Out Of Frame, FERF, Red Alarm, AIS, Idle
Error Counters: LCV, Framing errors, P-bit errors, CP-bit errors, FEBE, Excessive Zeros.

DS3 Data Channels

Supported channels: FEAC, Path Maintenance Data Link
FEAC: Send and receive Block Oriented Codes
Data Link: Send and receive HDLC formatted messages



Buyers Guide:

[UT301/302](#) - T3T1/T3E1 Analysis card with basic software

[SA000d](#) - High Stability Internal Clock Option

Optional Software

[UT3001](#) - FEAC Transmit and Receive

[UT3002](#) - Maintenance Facility Data Link

[UT3003](#) - API Development Toolkit

